Dr. Surendra Rathod
Professor, Electronics Department,
Sardar Patel Institute of Technology

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- **Date of joining the present institute: 01/10/1999**
- **Date of joining the present department: 01/10/1999**

- **Scholastic record: (*Begin with the highest degree and end with XII*)**

S.No	Degree	Institute	Year of passing	Class/CGPI/percentage
1	Ph.D.	IIT Roorkee	2011	--
2	M.E.	VJTI	2006	Distinction
3	B.E.	CoE Badnera	1997	First
4	H.Sc.	Shree Shivaji Science College Amravati	1993	First

- **Teaching/Industry experience in totality :**

  1) Working as **Professor of Electronics Engg.** in **Sardar Patel Institute of Technology, Andheri (West), Mumbai** since Feb. 2012. **(Approved from 29/07/2013)**
  2) As a **Ph.D. Research Scholar** in **Indian Institute of Technology Roorkee,** from Aug. 2008 to June 2011.
  3) As assistant professor in Sardar Patel Institute of Technology, Andheri (West), Mumbai since 1st June 2007. **(Approved from 19/01/2009)**
  4) As a Sr. Lecturer in **Sardar Patel Institute of Technology, Andheri(W), Mumbai** since 1st Aug 2006.
  5) As a Lecturer in **Sardar Patel College of Engineering, Andheri(W), Mumbai** since 1st Oct 1999.
  6) As a Lecturer in **F.C.R.I.T., Vashi,** from 9-3-1998 to 24-9-1999
  7) As a Lecturer in **KES College of Engineering, Pen, Raigad.**
  8) As a Visiting Lecturer in **Government Polytechnic, Pen, Raigad.**
  9) As a Quality control Engineer in **Finolex Industries Ltd., (Urse Division Pune)**

- **Achievements: --**

- **Awards:**

1) S. S. Rathod received recognition as IUCEE (Indo Universal Collaboration for Engineering Education) Faculty Fellow for the year 2016.

2) S. S. Rathod was awarded as a **Distinguished Professor by Computer Society of India (CSI)** for successfully demonstrating innovative and outstanding teaching methodology, organized by **IITB,** 2017.

3) S. S. Rathod was awarded as a **Distinguished HOD by Computer Society of India (CSI)** for successfully demonstrating innovative and outstanding teaching methodology, organized by **IITB,** 2017.

4) Received **'ISTE Best Engineering College Teacher Award for Maharashtra State"** in year 2012.

5) Received **'Shiksha Rattan Award' and 'Certificate of Excellence"** in year 2012 by International India Friendship Society, New Delhi

6) Received **'Outstanding Achievement Award'** for year 2007 by **Energy Society of India and College of Engineering Pondicherry by his Excellency, Government of Pondicherry**.

7) Won **First Prize** for the Paper Titled "Single Event Upset Study of Helium and Argon on P+/EPI/N+ and SRAM Structure" in the **national conference** held at Mumbai on 14th March 2009**.**

8) Won **Best Paper Award** for the Paper Titled "VLSI Implementation of a Viterbi Decoder" in the **national conference** held at **Government College of Engineering,** Aurangabad on 23rd & 24th Jan 2006.

9) Won **Best Paper Award** for the Paper Titled "Design and Simulation of PC to SRAM Interface for Reconfigurable Processors" in the **national conference** held at **MIT,** Manipal on 11th & 12th Nov 2005.

10) Prize winner in Project/Competition by ***Institution of Engineers(India)*** held at Nagpur on 16th and 17th March 1997. **(Project Title: Code Conversion, Arithmetic & Logical Operations in 'C')**

- **Domain expertise and areas of interest:** VLSI Design

- **Details of subjects taught:**

S.No.	Name of subject	Year and branch
1.	Analog CMOS VLSI Design	Final Year: ETRX
2.	Human Health Systems Approach	Second Year: ETRX, EXTC, COMP, IT
3.	Law for Engineers	Third Year: ETRX, EXTC, COMP, IT
4.	ASIC Verification	Final Year
5.	VLSI Design	Third Year
6.	IC Technology	Final Year

- **Workshops/Refresher courses/Training programs/Seminars attended:**

1. Completed Four Week NPTEL online course with Examination on '***Outcome Based Pedagogic Principles For Effective Teaching***' 23rd Jan – 17th Feb 2017 [Top 2% in India (95% result) Elite +Gold Medal Category]
2. Completed Twelve Week NPTEL online course with Examination on '***Twelve Week NPTEL online course with Examination on 'Digital VLSI Testing***' 23rd Jan – 14th Apr 2017 [Elite Category]
3. Completed Twelve Week NPTEL online course with Examination on '***VLSI Physical Design***' 23rd Jan – 14th Apr 2017
4. Attended One week training program on ***VLSI Design Flow using Xilinx Vivado targeting Xilinx 7-series FPGA and Zynq SoC architecture*** conducted by Coreel Technologies Sandeepani School of Embedded System Design Bengaluru from 6th-10th Sep 2016
5. Attended One week ISTE STTP on ***CMOS, Mixed Signal and Radio Frequency VLSI Design*** organized by IIT Kharagpur from 19th - 23rd Sep 2016.
6. Elsevier Connect Seminar on 7 Nov 2017 in Mumbai.
7. Attended workshop on COMSOL Multiphysics Simulation Tool on 10th June 2016 conducted by COMSOL Mumbai.
8. Attended One Week ***INUP Hands-on training on Nanofabrication Technologies*** during 19-23 Jan 2015 at IIT Bombay.
9. Attended 3 Days ***2nd INUP Familiarization Workshop on Nanofabrication Technologies*** during 28-30 Nov 2014 at IIT Bombay.
10. Attended 2 Days workshop on ***TI MCU Design Days 2014*** by Texas Instruments Bangalore on 9th and 10th Dec. 2014 at Mumbai.
11. Attended 2 days post conference tutorial on "**Low Power Embedded Systems using MSP430 Microcontroller**" organized by Texas Instruments India University Program during 6th and 7th April 2013.
12. Attended 1 week ISTE approved STTP on "**Design, Testing, Performance Evaluation & Applications of Microwave Antennae**" organized by VIT Pune on 18th to 22nd Dec. 2012.
13. Attended 2 days national workshop on AAkash organized by I.I.T. Bombay on 10th and 11th Oct. 2012.
14. Attended **2 weeks** ISTE approved STTP on ***"Embedded Digital Signal Processing"*** at S.F.I.T. from 5th June 2006 to 16th June 2006.

15. Attended **2 weeks** ISTE approved STTP on ***"Embedded System Design : A Unified Hardware / Software Approach"*** at K. J. Somaiya College of Engineering from 13th June 2005 to 24th June 2005.
16. Attended **1 week** workshop on ***"Microsoft.NET Train the Trainer Program"*** at S.P.C.E. from 14th June 2004 to 18th June 2004.
17. Attended Course in ***"Advanced VLSI Design"*** at ***M.S. Ramaiah School of Advanced Studies, Bangalore*****,** from 14th July to 19th July 2003.
18. Attended Postgraduate level course IT-606 on **"*Embedded Systems"*** under Distance Education Program at ***Indian Institute of Technology, Bombay***, from 8th Jan to 2nd May 2003 in credit mode.
19. Attended 3 days course on ***"UML & Rational Rose"***, jointly organized by S.P.C.E. and Rational Rose Inc. during 29th – 31st Jan. 2003.
20. Attended ***"Certificate Course in VLSI Design"*** at ***Bit Mapper Integration Technologies Pvt. Ltd. Pune*** from 9th Dec 2002 to 15th Dec 2002.
21. Participated in one day workshop on ***"VLSI Design with VHDL"*** at Thadomal Shahani Engineering College, Mumbai on 14th Sep. 2002.
22. Participated in DTE, M.S. approved **5 weeks** winter school on ***"Object oriented programming in C++ and Java"*** from 27th Nov. to 29th Dec. 2000 at S.P.C.E.
23. Six month part time course at ***Pentasoft Technologies Pvt. Ltd*** *(Andheri)* in 2000.

    (Java, Perl, CGI, HTML, Advanced Java)
24. One year part time *'ACD' Exports diploma* from ***Boston's Computer Institute*** *(Ghatkopar)* in 1998-1999. *(C, C++, VB 6.0, VC++, Oracle, Developer 2000)*
25. Participated in one week Linux Administration course at SPIT in July 2008

- **Workshops/Refresher courses/Training programs/Seminars conducted as a resource person:**

1. Invited to conducted two day session on 'Accreditation' by Viva Engineering College on 17-18 June 2019.
2. Invited to conducted session on Innovative teaching learning methodologies by FCRIT Vashi on 24th June 2019.
3. Invited to conduct session on Autonomy by D. J sanghavi Engineering College on 28th June 2019.

4. Resource Person for Session on Active Teaching Learning Strategies Using Innovative Technology on 25/02/2019 at DJSCE, Vile Parle

5. Resource Person for STTP on "Flipped Classroom and MOOCS" 6th Feb 2019 at Agnel Polytechnic

6. Invited to deliver expert talk on 'VLSI Applications' by RGIT Versova on 6 Feb 2018.

7. Invited for expert talk on 'Research Methodology' June-July 2018 during ISTE approved five day FDP at PVPPCoE, Chembur

8. Resource Person for sessions on "Analog VLSI Circuits" and "Verification" in IETE Approved one week STTP on 25th and 26th June 2018, SAKEC, Chembur

9. Resource Person for session on "Outcome Based Education and NBA Process" on 12/07/2018 during one week FDP at MIT Aurangabad

10. Invited to deliver expert talk on "Higher Education" Opportunities and Challenges" during Higher Education Day at Terna Engineering College on 16th Mar 2018.

11. Invited to deliver talk on "Academic Autonomy" by Vivekananda Engineering College Chembur on 24 March 2018

12. Invited to deliver expert talk on "Recent Trends in VLSI" by CRCE Bandra on 6thMar 2018

13. Resource Person for AICTE-ISTE Approved STTP on "Synergogy, ICT Enabled Teaching Learning and Accreditation" at Kalsekar Engineering College Panvel.

14. Invited for session on "Blended MOOCs with existing pedagogy" during workshop organized by CRCE Bandra in association with Thapar University, Patialaon 8 July 2017

15. Conducted workshop on "Innovative Teaching and Learning" at Vidyalankar Polytechnic Wadala on 9 Sep 2017

16. Invited for conducting Two Days sessions on 2-3 Apr 2018 during AICTE-ISTE approved STTP on "Accreditation Procedure: NBA and NAAC" organized by SSJCET Asangaon.

17. Invited as speaker IEEE-CRCE Student Branch Organized Seminar on 'Technical Paper Writing' on 05 Aug 2017.

18. Invited to deliver expert talk on 'Emerging trends on VLSI design' at PVPPCoE Chembur on 22 Sep 2017.

19. Conducted workshop on 'Outcome Based Education' at M. H. Saboo Siddik College of Engineering on 29-30 July 2016.

20. Conducted workshop on 'OBE and NBA' at SIES Engineering College in 2017.

21. Invited as resource person for workshop on 'VLSI and its industry relevance' at Atharva College of Engineering on 12/08/2016

22. Delivered seminar on "Need of Ethics in Research" at S.P.I.T. on 11th Nov. 2016.

23. Took two sessions during workshop 'MSP-FPGA Hardware &Software co-design' organized by EXTC dept. of S.P.I.T. on 16th-17th Sep 2016

24. Invited to deliver a talk on "Novel Multi-gate Semiconductor Technologies" during NCATM-2017 National Conference on 24 March 2017 at ACPCE Kharghar

25. Workshop on 'VLSI and its industry relevance' on 12/08/2016 at Atharva College of Engineering

26. Resource person for One Week STTP on "Outcome Based Education-Innovative Teaching Learning Practices and Evaluation" from 2nd May to 6th May 2016 organised by Electronics Engineering Department of S.P.I.T.

27. Resource person for Two Week FDP on "Analog CMOS VLSI Design" from 7th Dec to 12th Dec. 2015 organised by Electronics Engineering Department of S.P.I.T.

28. Resource person for Two Week FDP on "ASIC verification with System Verilog" from 21st to 26th Dec. 2015 organised by Electronics Engineering Department of S.P.I.T.

29. Conducted one day session on 'Outcome Based Education' under AICTE-ISTE approved STTP at Kalsekar Polytechnic Panvel on 14th June 2017. More than 80 teachers were in the audience.

30. Conducted three days workshop on 'Outcome Based Education' at Agnel Polytechnic Bandra on 23rd, 24th and 28th January 2017. More than 70 teachers were in the audience.

31. Resource Person for Webinar on 'Improvement in Laboratory Experiences in Engineering Education' organized by IUCEE. There was excellent worldwide attendance for this webinar and received good feedback from attendees.

32. Resource Person for one day seminar on 'Insights of outcome based education' at Indira Gandhi College of Engineering

33. Resource Person for one day seminar on 'outcome based education' at Atharva College of Engineering

34. Resource Person for two days workshop on 'VHDL and Verilog Programming' at Babasaheb Naik College of Engineering Pusad

35. Resource Person for two days workshop on 'Outcome Based Education' at SSPM College of Engineering Kanakavali
36. Invited talk on 'CMOS Analog VLSI Design' at SAKEC Chembur
37. Invited talk on 'Introduction to VLSI' at Prof. Ram Meghe Institute of Technology Badnera
38. Invited talk on 'CMOS Analog Electronics' at DBIT Kurla
39. Session Chair for International Conference at Dilkup College of Engineering
40. Session Chair for IEEE Bombay section Paper presentation contest at CRCE Bandra
41. Session Judge for IET PATW Event at Sardar Patel College of Engineering
42. Resource person for one day seminar on "NBA Accreditation" at D. J. Sanghavi College of Engineering, Mumbai on 16th Sep 2015.
43. Resource person for STTP on 'Accreditation Process" at Vidyavardhini College of Engineering Vasai on 19th Aug. 2015.
44. Resource person for STTP on 'Accreditation Process" at Karmveer Bapurao Patil Engineering College Satara on 22nd Jun. 2015.
45. Resource person for STTP on 'Outcome based education' at Kalsekar Polytechnic Panvel on 11th Jun. 2015.
46. Resource person for one day seminar on "NBA Accreditation" at Amrutvahini Polytechnic on 11th Apr. 2015.
47. Resource person for Two day workshop on "Challenges in VLSI Design" at C.R.C.E. Bandra on 13th and 14th Mar. 2015
48. Resource person for one day seminar on "NBA Awareness Workshop" at L. T. College of Engineering on 27th Feb. 2015.
49. Resource person for one day seminar on "NBA Do's and Don'ts" at Theem College of Engineering, Palghar on 27th Dec. 2014
50. Resource person for one day seminar on "Outcome Based Accreditation Process" at Bharti Vidyapeeth College of Engineering on 16th Dec. 2014
51. Resource person for one day session on "Attainment of course outcomes" for one week workshop on "Outcome based accreditation" at Fr. C.R.C.E. Bandra on 18th Nov. 2014

52. Resource person for session on “CMOS Analog VLSI Design” for ISTE approved one week STTP on “An insight into VLSI and Nanotechnology” at Shah and Anchor College of Engineering on 17th July 2014
53. Resource person for session on “Research Analysis” for two week Faculty Development Programme on “Research Methodology for PhD Aspirants” at K.J.S.C.E. Sion on 6th May 2014
54. Resource person for workshop on “NBA accreditation outcome assessment” at FCRIT Vashi on 31st June 2014
55. Resource person for session on “ CMOS Analog VLSI Design” and “Mixed Signal VLSI Design” for the AICTE Sponsored National level STTP on "VLSI and Embedded Systems" at F.C.R.I.T. Vashi on 2nd July 2013
56. To motivate teachers of Mumbai university for research a guest lecture on Technical Paper Writing was taken in July 2011.
57. To motivate students to design electronic circuits with a VHDL a guest lecture at Khurana Sawant Institute of Technology was taken in Aug 2011.
58. To motivate teachers at Rajaram Mane College of Engineering for research delivered lecture on how to write a technical paper was taken in Jan 2012.
59. To motivate students and teachers of engineering colleges to increases interaction with industry a guest lecture on “Mentor Graphics VLSI Tools” in association with Techlabs Pune was taken in Jan 2012.
60. To motivate students of engineering colleges to write research paper a seminar on ‘Technical Paper Writing’ was taken. It was organized by Forum for Aspiring Computer Engineers’ (FACE) in Feb 2012.
61. To share technical aspects of radiation effects on integrated circuits on electronic devices and circuits a presentation to world wide CISCO engineers was delivered through webex in association with CISCO San Francisco USA.
62. To explore students and teachers to latest trends in VLSI a guest lecture on ‘Scaling Issues and Solutions for MOS devices’ was delivered at FCRIT Vashi on 22nd Feb 2012.
63. A guest lecture on ‘Reliability of MOS Devices and Circuits’ was delivered at VIT Mumbai on Mar 2012.
64. An invited talk on ‘Issues in Design of High speed communication circuits’ was delivered at IETE Zonal Seminar (West), Vashi on 5th May 2012.

65. Conducted lectures for two days for teachers of Electrical Engineering of SPCE on 'Digital System Design' organized under TEQIP in Aug 2012.
66. To train students of SPCE an invited talk on 'VHDL' was delivered. It was organized by Electrical Engineering Students Association (EESA) on 27th Sep. 2012

- **Membership of professional bodies:**

IEEE Senior Member (Member (90509971)
FSAI Member (1803433): FSAI Bombay Section Student Chair
ISTE Life Member (LM-32960)
ISNT Life Member (LM-5968)

- **Publications:**

International Conferences (Latest five are shown below out of 50 conference papers**)**

S.No	Publisher	Title of International conference	Title of paper/article/poster presentation	Schedule and venue of conference
1.	IEEE	*Int. Conf. on Communication, Information & Computing Technology (**ICCICT 2018**)*	Mutual Coupling Reduction in Patch Antenna Using Electromagnetic Band Gap (EBG) Structure for IoT Application	Mumbai, India, 2nd – 3rd Feb. 2018
2.	IEEE	*Int. Conf. on Communication, Information & Computing Technology (**ICCICT 2018**)*	Implementation of MRI Gradient Generation System and Controller on Field Programmable Gate Array(FPGA)	Mumbai, India, 2nd – 3rd Feb. 2018
3.	IEEE	*Int. Conf. on Intelligent Computing and Control (**I2C2**)*	An Automated Antenna Pattern Measurement System	Coimbatore, India, 23rd – 24th June 2017
4.	VLSI Society of India	21st Int. Symposium on VLSI Design and Test (VDAT)	Synapse circuits Implementation and Analysis in 180nm MOSFET and CNTFET technology	IIT Roorkee, June 2017
5.	IEEE	Int. Conf. on Communication and Electronics Systems (ICCES)	Analysis of Multifin n-FinFET for Analog Performance at 30nm Gate Length	Coimbatore, Oct 2016.

- **Details of National and International Journal publications:**

S.No	Title of Journal	Title of paper	Co-authors

1.	***Elsevier Microelectronics Journal***	SOI FinFET Based Instrumentation Amplifier for Biomedical Applications	Reena Sonkusare and Omkar Joshi
2.	***IEEE Trans. on Antennas and Propagation***	A Compact Dual Band Gap Electromagnetic Band Gap Structure	Pramod P. Bhavarthe and K. T. V. Reddy
3.	***IEEE Computer Society VLSI Circuits and Systems Letter***	Design and analysis of SOI FinFET Based Three Stage OTA with Nested Gm-C Frequency Compensation	Reena Sonkusare, P. Pilankar, A. Gosavi and K. Sutar
4.	***Springer Analog Integrated Circuits and Signal Processing***	Analysis of subthreshold SOI FinFET based two stage OTA for low power	Reena Sonkusare and P. Pilankar
5.	***IEEE Microwave and Wireless Components Letters***	A Compact Two Via Hammer Spanner type Polarization Dependent Electromagnetic Band Gap Structure	Pramod Bhavarthe and K.T.V. Reddy
6.	***IEEE Computer Society VLSI Circuits and Systems Letter***	Simulation and Analysis of analog VLSI Silicon Neuron using Carbon Nanotube Field Effect Transistor and 180nm MOSFET Technology	Sushma Srivastava
7.	***IEEE Computer Society VLSI Circuits and Systems Letter***	Design of SOI FinFET based Two Stage Operational Transconductance Amplifier	Reena Sonkusare, P. Pilankar and A. Saini
8.	***IEEE Microwave and Wireless Components Letters***	Parametric Study for Rectangular Patch Antennas	Pramod Bhavarthe and K.T.V. Reddy
9.	***Indian Journal of Technical Education***	Simulative study of a novel MEMS cantilever design using CoventorWare	Karan Shah, Gauri Dalvi, Samiksha Gupta and Prashant Kasambe
10.	***IETE Journal of Education***	Investigation of Electromagnetic Radiations in Mumbai	--
11.	***IET Circuits, Devices and Systems***	Analysis of Double-Gate FinFET Based Address Decoder for Radiation Induced Single-Event-Transients	A. K. Saxena, and S. Dasgupta
12.	***Journal of Active and Passive Electronic Devices***	Study of Quantum and Classical Transport in 25nm Omega FinFET under Gamma Radiation: 3D Simulation Study	A. K. Saxena, and S. Dasgupta
13.	***Wiley Interscience Journal of Circuits, Systems, and Computers (JCSC)***	DG-FinFET based SRAM Configurations for Increased SEU Immunity	A. K. Saxena, and S. Dasgupta
14.	***IETE Technical Review***	Radiation Effects in MOS Based Devices and Circuits: A Review	A. K. Saxena, and S. Dasgupta
15.	***Elsevier Microelectronics Reliability***	A Low Noise, Process-Variation-Tolerant Double-Gate-FinFET based Sense Amplifier	A. K. Saxena, and S. Dasgupta

16.	***ASP Journal of Low Power Electronics***	Robust Double Gate FinFET based Sense Amplifier Design Using Independent Gate Control	A. K. Saxena, and S. Dasgupta
17.	***Elsevier Microelectronics Journal***	Electrical Performance Study of 25 nm Ω-FinFET under the Influence of Gamma Radiation: A 3D Simulation	A. K. Saxena, and S. Dasgupta
18.	***IET Circuits, Devices and Systems***	Alpha Particle Induced Effects in PD-SOI Device: With and Without Body Contact	A. K. Saxena, and S. Dasgupta
19.	***Elsevier Microelectronics Reliability***	A Proposed DG-FinFET based SRAM cell Design with RADHARD Capabilities	A. K. Saxena, and S. Dasgupta
20.	***IEEE Trans. on Electron Devices***	Radiation Effects in Si-NW GAA FET and CMOS Inverter: A TCAD Simulation Study	Gaurav Kaushal, Satish Maheshwaram, S. K. Manhas, A. K. Saxena, and S. Dasgupta
21.	***IEEE Trans. on Electron Devices***	Comparative Analysis of SEU in FinFET SRAM Cell's for Super-Threshold and Sub-Threshold Supply Voltage Operation	A. K. Saxena, and S. Dasgupta
22.	***AIP Journal of Applied Physics***	Modeling of Threshold Voltage, Mobility, Drain Current and Sub-threshold Leakage Current in Virgin and Irradiated Silicon-on-Insulator Fin-Shaped Field Effect Transistor Device	A. K. Saxena, and S. Dasgupta
23.	and many more……		

- **Details of Book Chapters Published:** "Radiation hard circuit design: flip-flop and SRAM " chapter 12 in IET book "VLSI and Post-CMOS Electronics. Volume 2: Devices, circuits and interconnects" authored by Gaurav Kaushal ; Surendra S. Rathod ; Ch Naga Raghuram ; Sudeb Dasgupta doi:10.1049/PBCS073G_ch12

- **<u>R& D and Consultancy</u>:**

<u>Grant Received:-</u>

1. Mumbai University Minor Research Grant of Rs. 30,000/-- for the project "Determination of Water Quality Parameters" in year 2016-17.

2. Mumbai University Minor Research Grant of Rs. 35,000/-- for the project "Labview Based Online Pressure Monitoring System" in year 2013-14.
3. AICTE grant of Rs. 6.9 Lakhs for FDP on 'Electronic System Design: From devices to applications' in year 2014-15.
4. AICTE grant of Rs. 1 Lakh for National Seminar on 'Technologies for Development of Rural Areas' in year 2017-18.
5. AICTE-ISTE grant of Rs. 3 Lakhs for FDP on 'Innovative Teaching Learning Practices to Achieve Outcome Based Education and Accreditation' in year 2017-18.
6. AICTE grant of Rs. 3.62 Lakhs for STTP on 'Front End VLSI Design and Verification' in the Financial year 2018-19.
7. AICTE grant of Rs. 5.32 Lakhs for FDP on 'Consumer Electronic Product Design, Testing, Reliability and Patenting' in the Financial year 2018-19.

Ph.D. Guidance:-

1. Approved Ph.D. guide of Mumbai University for Electronics Engineering since 2015.
2. Approved Ph.D. guide of Mumbai University for Electronics & Telecommunication Engineering since 2013.
3. **Ph.D. Guided: Total=03**

Name of Research Scholar	Title of Ph.D.	Year of Completion
Mr. Pramod Bhavarthe	Design of Compact Electromagnetic Band Gap Structures for Enhancement of Microstrip Patch Performances	2019
Mrs. Reena Sonkusare	Analysis of FinFET for analog performance and its application in analog circuit	2019
Mrs. Sushma Srivastava	Modeling of CNFET Based Neuromorphic Circuits	2019

4. **Present Research Scholars: Total=06**

S.N.	Name of Research Scholar	Title of Ph.D.
1	Mrs. Manisha Bansode	Design of Compact Monopole Antenna with Low Specific Absorption Rate using Metamaterial

2	Mrs. Payal Shah	Modeling and Design of Silicon Neurons and Synapse for Neuromorphic Chip Implementation
3	Mr. Vijay Kapure	Design of Metamaterial Structure for Triple Band-notch Ultrawideband Monopole Antenna
4	Mrs. Vidya Keshwani	Design of Compact Monopole Antenna with Low Specific Absorption Rate using Metamaterial
5	Mr. Shrikant Velankar	Not yet finalized
6	Mr. Kumar Khandagale	Water Quality Monitoring

- **Contribution to Corporate life and management of the Department and Institution:**
    - **Head of Electronics Department from Nov 2011 to Sep 2019**
    - **Dean of Academics from Jan 2017 to Sep 2019**
- **Other Contributions:**

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