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Technology Migration: From Microelectronics to Nanoelectronics

(*Invited)*

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Moore's Law, an historical observation, in 1965, by Intel executive, Gordon Moore, that the functionality per chip (bits, transistors) doubles every 2 years. The performance increases by the device shrinking within a given volume to decrease the power consumption and to decrease cost per unit chip. Moore's Law is used to improve the economic growth of semiconductor technology. A vision of the future for scientists and engineers to makes it all possible. According to the ITRS-2006, gate length down to 32 nm in 2007 and 6 nm around 2020.

Nanoelectronics is concerned with understanding and exploiting the properties of devices which have dimensions at the nanometer scale. The drive for ever smaller dimensions in the semiconductor industry has made the design issue for such devices one of the prime area of study. Theoretical modeling has suggested that conventional single-gate MOSFETs may operate down to channel lengths of 30 nm. Using double-gate MOSFETs, channel lengths below 10 nm may be achieved. For Terabit/chip technology radical alternatives to CMOS are needed and should be available by 2012 to avoid a dislocation in progress. Single electron tunneling (SET) devices are perceived by some to be the natural successor to the MOSFET. For CMOS structures, reduced voltage operation is obvious to reduce power consumption. In coming era, larger trade-offs are to be dealt with as far as low power design is concerned. The trade off might be larger layout, unequal noise margins etc. Surely, the future of semiconductor industry is expected to see a sea change in basic design as well as fabrication principles.