Timing Analysis of ITU G.707 Based VDOS (voice and data over SDH) Receiver Using VHDL

Sunanda Manke , Kavita Khare and S.D. Sapre

Abstract---**SDH is the transport technology standardized in 1990 by ITU for optical transmission. It is a TDM based technology, which was optimized for voice transmission, when came in to existence. For achieving data connectivity in wide area network, new technologies were developed to insert data in SDH frame. It resulted in efficient data transmission using SDH through the network infrastructure already laid for voice transmission. This saved the cost of laying new infrastructure for data transport. The technologies used for this purpose were GFP for encapsulating the data, VCAT to insert data in to SDH frame and LCAS for resizing the bandwidth. VCAT combines number of virtual containers, together called as virtual containers group (VCG) resulting in right sized pipe for data transmission. LCAS can dynamically increase or decrease number of virtual containers hitlessly, resulting in resizing the BW between two end points as per the traffic requirement. Generally one VCG contains the same type of signal either voice or data but it is possible to transmit both voice and data together in one VCG, which will result in less hardware requirement and lower cost.**

This paper describes the design of a receiver circuit used to receive both voice and data signal transported in the same VCG. The VCG receiver separates 10mbps Ethernet data and PCM-30(2Mbps) voice signal from VCG containing VC-12 containers (VC12-6V) as a case. All members of VCG traverse through different path to reach the destination. This results in differential delay at the receiver and buffer is required at the receiver to cater this delay. The size of the buffer decides the differential delay compensation. The receiver in this paper compensates for 64 ms differential delay. The design can be extended for higher rate voice and data signal by changing the buffer size at the receiver. Coding of receiver is done in VHDL and the platform used for simulation is Modelsim

Index Terms-- **GFP-Generic Framing Procedure, LCAS-Link Capacity Adjustment Scheme, SDH- Synchronous Digital Hierarchy, , STM - Synchronous Transfer Mode , VCAT-**

Virtual Concatenation, VCG-Virtual Concatenated Group, VC-Virtual Container

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I. Introduction

A. Voice over SDH

SDH was designed and optimized for voice transmission through optical link. It is a TDM technology designed to multiplex bit flows into larger flows. It uses specific frame format to carry data plus overhead bytes. The frames are called STMs in to which VCs are packed. SDH channels are synchronous and synchronization is supported by pointer bytes, which detects the initial byte position of each container. Table I gives the data rate at different hierarchical levels of SDH/SONET and number of E1 channels (2mbps) supported at each level.

TABLE I
SDH/SONET RATES

Optical Level	SONET Electrical Level	SDH Equalvalent	Line Rate (Mbps)	Payload Rate (Mbps)	Overhead Rate (Mbps)	SONET Capacity	SDH Capacity
OC-1	STS-1	-	51.840	50.112	1.728	28 DS-1s or 1 DS-3	21 E1s
OC-3	STS-3	STM-1	155.520	150.336	5.148	84 DS-1s or 3 DS-3s	63 E1s or 1 E4
OC-12	STS-12	STM-4	622.080	601.344	20.736	336 DS-1s or 12 DS-3s	252 E1s or 4 E4s
OC-48	STS-48	STM-16	2488.320	2405.376	82944	1344 DS-1s or 192 DS-3s	1.008 E1s or 16 E4s
OC-192	STS-192	STM-64	9621.504	331.776	331.776	5376 DS-1s or 192 DS-3s	4.032 E1s or 64 E4s

B. Data over SDH

Demand of data traffic in Wide area network is increasing day by day. Connectivity for data traffic can be achieved either by laying new infrastructure for data transmission or by using already laid SDH infrastructure. Technologies are developed and standards are defined for proper transmission of data over the SDH network.

Three steps are required to make the data fit into the SDH Frame i.e. to transmit data over SDH links as shown in the fig 1 [6],[7],[8],[9].

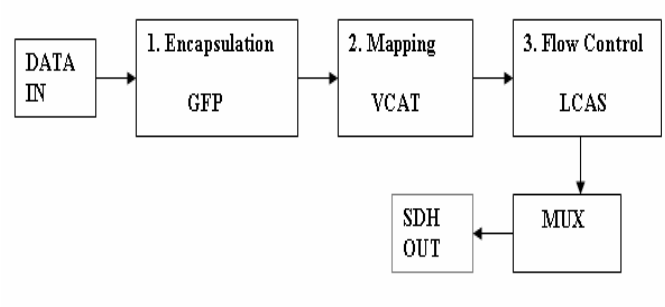


Fig.1 Data over SDH

1) Encapsulation

Framing protocol is required to encapsulate data packet to generate SDH payload. Most commonly used protocol is GFP[5].

2*) Mapping*

After encapsulating the data using GFP, it is concatenated. Concatenation is the process of integrating several containers to a unified one to provide a larger tunnel for transportation. There are two kinds of concatenation, contiguous concatenation and virtual Concatenation. From the perspective of technological and economical feasibility VCAT is preferred [3].

VCAT is a standardized layer 1 inverse multiplexing technology that can be applied to the OTN, SONET/SDH, PDH component signals. It breaks the integral payload into individual containers, separately transports each container and recombines them to a contiguous bandwidth at the end point of the transmission. The number of containers used is user specific i.e. it depends on the data rate to be inserted in SDH frame. The group of VCs used is called a VCG. Individual member of VCG can traverse through any path to reach the destination and all VCs are combined at the destination as per the MFI (Multiframe Indicator) and Sequence Number written in the control packet of the frame [1]. Only the path originating and path terminating equipment need to recognize and process the virtually concatenated signal structure. Intermediate nodes can remain entirely unaware of this fact. Thus, only edge equipments hardware need to be made compatible with the VCAT technology. As VCG members travel through a different path to reach destination, they arrive at different times at the destination. This differential delay needs special provision made at the receiver.

Table II shows the VCAT for SDH signals, maximum number of signals allowed and the data rate it can achieve [1].

TABLE-II
VCAT TYPE AND DATA RATE

VCAT type	Component Signal	X- Range	Capacity(Kbps)
VC-11 XV	VC-11	1to 64	1600 to 102400
VC-12 XV	VC-12	1to 64	2176 to 139264
VC-2 XV	VC-2	1to 64	6784 to 434176
VC–3 XV	VC-3	1to256	48348 to12.5Gbps
VC-4 XV	VC-4	1to256	149760to 38.3 Gbps

To understand the table ,let us take an example of transmitting 100Mb Ethernet data using SDH, we can either go for VC-3 2V or VC-4 1V or VC-12 50V to achieve the desired data rate.

3) Flow Control

Flow control is required for dynamic bandwidth allocation as the data rate can vary. The protocol used for flow control is LCAS (link capacity adjustment scheme). LCAS enhances the VCAT scheme with hitless in service addition and removal of VC's to/from the VCG. Additionally LCAS provides load sharing protection by dynamically removing failed members from the VCG when they experience fault and as the fault is repaired, the member can again be added to achieve the normal flow. The combination of VCAT and LCAS is a very powerful addition to the SDH standard as it solves the bandwidth granularity problem. In fact, they increase the value of existing SDH networks by allowing bandwidth efficient scheme of new services [4]. After LCAS, signal goes to MUX block where it is multiplexed with other containers/STM's for transportation through SDH link.

II. VOICE AND DATA OVER SDH (VDOS)

VDOS is the technology proposed for simultaneous transmission of voice and data in the same VCG group. This is achieved using VCAT technology. The VCG has specific number of VCs carrying information. For simultaneous voice and data transmission, in one VCG group, the VCs can be distributed between voice and data. As per the data rate requirement, data traffic can be mapped into specific number of virtual containers. The remaining containers can be used for voice traffic as the maximum capacity of a VCG is quite high compared to the bandwidth required for the data traffic. VCAT is used for generating VCs for data traffic as well as voice traffic.

Table III shows the different types of data traffic transported using SDH ,types of VCG used with number of virtual containers required [3] ,capacity of VCG ,the number of E1(2Mbps i.e. PCM 30 voice channels) channels that can be supported and the total data rate.

TABLE III
VDOS RATES

Type of data	VCAT Component	Capacity of VCG	No. of E1 channels (voice)	Total data rate(Mbps)
Ethernet 10 Mbit	VC-12 5V	1 to 64	1 to 59	11.20 to 143.360
Fast Ethernet 100 Mbit	VC-12 46V VC-3 2V	1 to 64 1 to 256	1 to 18 1 to 40704	103.040 to 143.360 97.92 to12.53Gb
Gigabit Ethernet 1000Mbit	VC-3 21V VC-4 7V	1 to 256 1 to 256	1 to 3776 1 to 15687	1028.16 to 12.53Gbps 1052.31 to 38.3 Gbps

III. IMPLEMENTATION

Receiver block is designed to receive Ethernet data of 10 Mbps and PCM-30 voice signal (2Mbps) simultaneously using VCAT.VC-12 is the container used for transmission. As the data rate of VC-12 is 2240Kbps, total VCAT Capacity required is VC-12 6V, where 5V is used for data and 1V for the voice transmission. Thus six serial streams of VC-12 are input to the receiver. The function of the receiver is to extract data (Ethernet) and voice (PCM) signals from these streams. As all the streams travel through different path to reach the destination. They reach at the receiver at different point of time. These streams need synchronization before extracting the data from them. The transmitter inserts sequence number in the frame, which is extracted at the receiver from each stream and matched for the synchronization [2],[10],[11]. Fig 2 shows the block diagram of receiver.

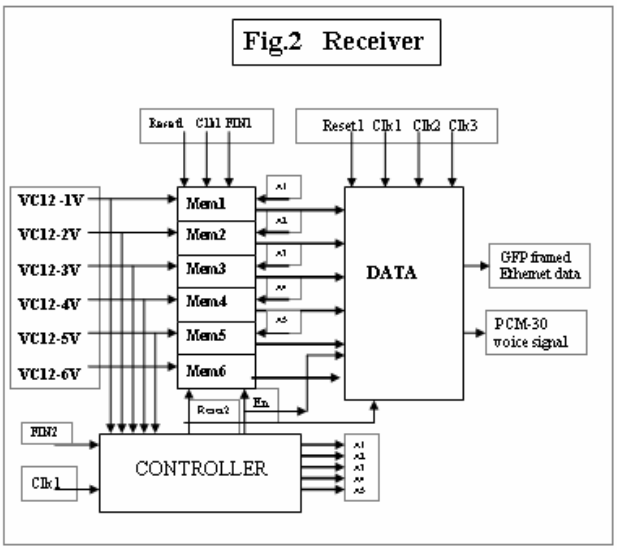
Input - Inputs to the receiver are six VC-12 streams and two synchronization pulse (FIN1 & Fin2) to indicate the location of V5 byte and the sequence number respectively in the VC-12 multiframe. Three clock signals are required to input and output the data at different points.

Clk1 is used to input the VC-12 streams. Its data rate will be 2240kbps.Clk2 outputs Ethernet data.Clk3 is used to output E1 signal.

Output - The output of this block is GFP framed Ethernet data and E1 (2Mbps) signal.

MEMn(1 to6) - Number of memory elements depends on the number of members of a VCG group (here it is 6).the size of each memory unit depends on the maximum differential delay to be compensated and maximum possible value here is 64ms and the size required here is 128x35x4=17920byte.

Controller - Controller extracts and stores sequence no. of each incoming stream, simultaneously it compares them to find the match, as soon the match is found it gives enable signal (EN) and address for each memory (A1, A2…) corresponding to the same sequence number. The output of all the memories are synchronized (i.e. streams having same sequence number are outputted), thus they can be combined together by the **Data Block** to give the data in the form of framed Ethernet data. Also, voice sequence number is checked separately and corresponding output is given to **Data block** which then gives the E1 signal. The controller continuously checks the sequence number and keeps enable signal high if sequence number matches .But if at any point of time there is a mismatch in the sequence number then it disables the EN signal and resets(reset2) all memories and starts the whole process again. In the Synchronous mode, if memories become full, the data is overwritten but if Synchronization is not achieved in the cycle of 64ms, then controller issues the reset signal (Reset2) to all memories to clear them.



IV. SIMULATION RESULTS

Fig 3 shows the receiver input and output streams.**din1** to **din6** are the input streams(VC12) in which five streams contain data and the sixth stream is the PCM data.**dout1** is the output Ethernet data and **dout2** is the output PCM data.**fin1** indicates the start of the incoming stream. Input data is received at clock rate of **clk1**, out1 is obtained at **clk2** and out2 at **clk3**

Fig 4 shows the memory block with inputs and corresponding output. Six memory blocks are used in the design for six input streams. Each block takes input data on pin **din** at the clock rate of **clk1**.fin1 indicates the start of input data. Rest is the reset signal. Data on **dout** starts after **en** goes high, which the signal is given by the controller after all the streams are synchronized. **add** signal also given by the controller indicates the location from which the data is to be outputted.

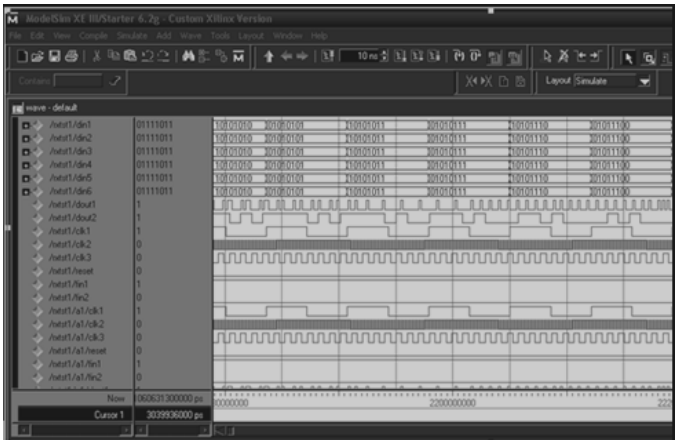


Fig. 3 Receiver Input Output Signals

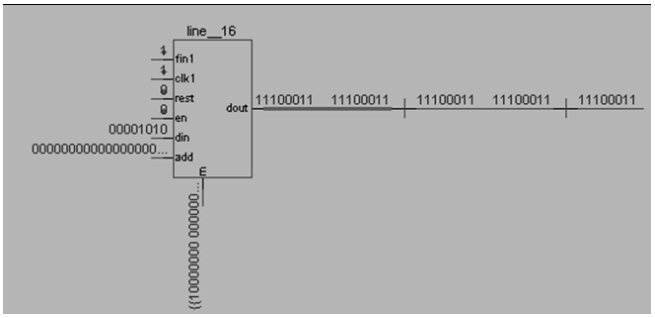


Fig. 4 Block diagram of memory block

Fig 5 shows the input and output waveforms of memory block. It continuously inputs the data and as soon it gets **en** signal from controller block, it takes the address from the **add** line starts outputting the data from the specific location.

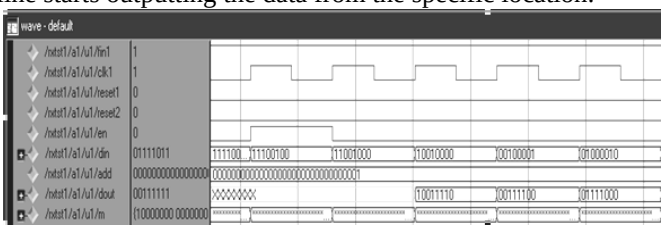


Fig. 5 Input and Output Waveforms of memory block

Fig 6 shows the content of memory in the memory block. The address obtained from the controller block on **add** line is "001", which means that the data should be outputted from the 2nd frame i.e.140th location (as one frame is of 140 bytes [0-139]).The byte on 140th location is '10011110' .and the data on **dout** line starts with this byte as can be seen from the wave of **dout** line.

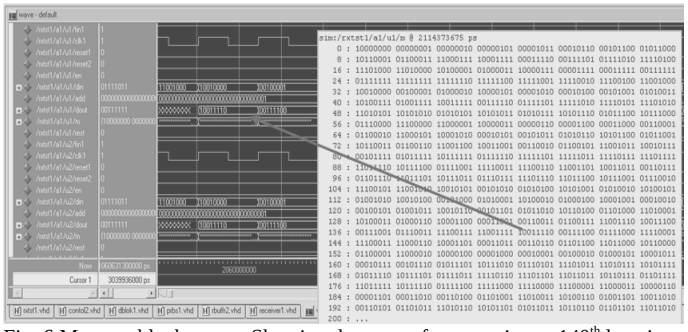


Fig. 6 Memory block output Showing dout waveform starting at 140th location of memory having data byte '10011110'

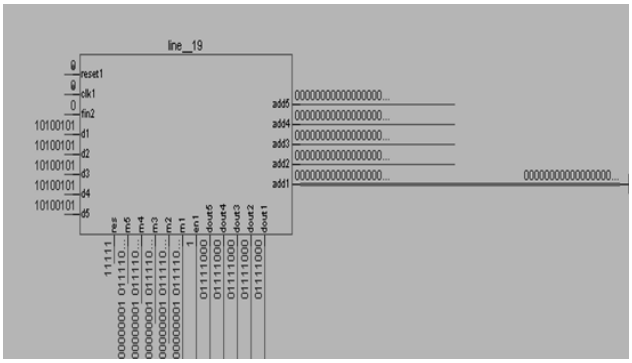


Fig .7 Block Diagram of Controller Block

Fig 7 shows the input and output signals of control block. This block takes the input data whenever fin2 is high and stores it in memory locations m1 to m5.it compares the memory locations for the specific byte and gives the output as addresses accordingly.

Fig 8 shows the waveforms of controller block.**d1** to **d5** are the input streams. **fin2** indicates the position of sequence number byte in the frame. Whenever **fin2** goes high controller block saves the byte in memories m1 to m5.it compares the individual memory byte for specific sequence number. For simulation purpose it is comparing with '01111000' and as soon it gets this byte in all memory locations ,it gives **en** high and the corresponding address on **add1** to **add5** lines as shown in fig 9.

Fig 10 shows the memory contents of m5,here '01111000' is obtained at 2nd location so it gives the address as '001'(000 is the first location) and **en** goes high for one clock cycle indicating that the synchronization is achieved.

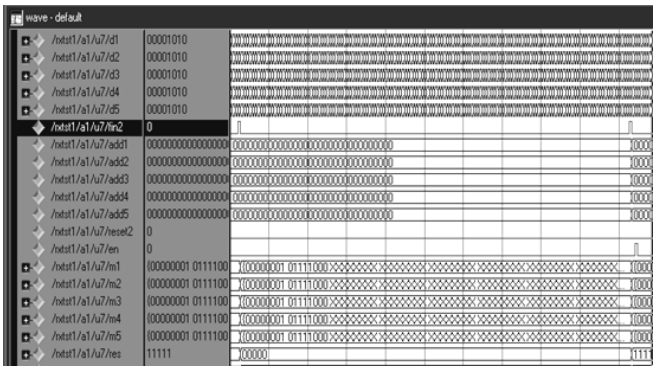


Fig. 8 Input and output waveforms of Controller Block

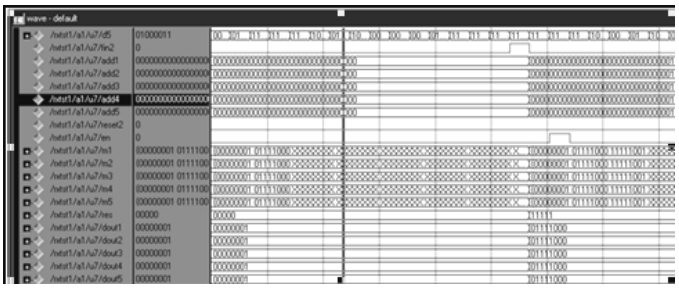


Fig. 9 Controller Waveforms showing 'en' High and corresponding values on 'add' lines

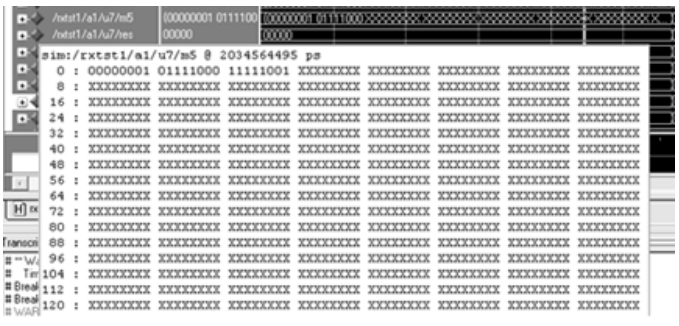


Fig. 10 Memory Content in Controller Block

Fig 11 shows the waveforms of data block. Input **din1** to **din6**

are obtained from the memory block. This block removes all overhead bytes and stuffing bytes and gives two output streams. **dout1** the Ethernet data at the clock rate of **clk2** and **dout2** PCM data at the clock rate of **clk3.**

Fig. 11 Data Block Waveforms

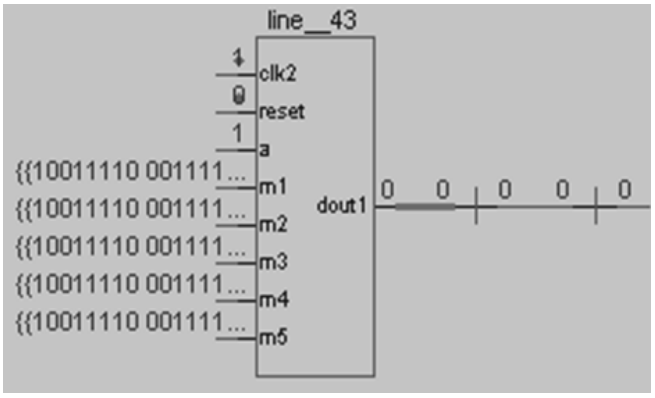


Fig. 12 Block diagram of Data Block for dout1

Fig 12 shows the formation of dout1 from memories m1 to m5.the 5 input streams of data block are stored in five memory locations and dout1 is the serial output data. It takes output from one memory at a time and takes data byte one by one from each memory and outputs at the clock rate of clk2.

Fig 13 shows the dout2 output which is taken from memory location m6 of data block directly. It outputs the data serially at the clock rate of clk3.

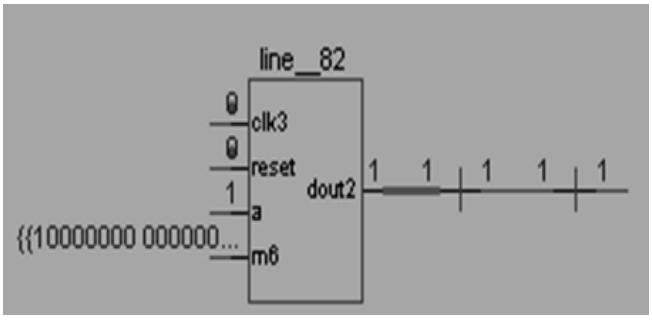


Fig 13 Block diagram of Data Block for dout2

V. CONCLUSION

In this paper, Virtual concatenation is utilized for both voice and data transmission simultaneously. The circuit described receives 10Mbps Ethernet data with PCM-30 (2Mbps) signal in one VCG of VC-12 containers. The same concept can be utilized for higher data and voice rates by using higher order virtual containers.

This paper gives simulation results of receiver circuit and verifies the functionality of the various blocks used.

The received streams are to be synchronized before generating the output streams as all the incoming streams traverse through different paths. The controller of the receiver circuit takes care of the synchronization using FSM. All the three blocks of the receiver circuit namely memory, controller and data block uses RAM to store the incoming stream. The size of the RAM in all the blocks is decided as per the incoming data rate and the differential delay compensation required (memory block). If we go for higher rates of the incoming data or more differential delay requirement, the RAM size will change.

VI. REFERENCES

Standards

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VII. BIOGRAPHIES

Sunanda Manke did her Graduation in electronics and communication engineering in 1992 and her Post graduation in digital communication in 2003.she worked in R & D division of M/S Optel Telecom Ltd. from 1993 to 1999 before joining University institute of technology, Barkatullah university, Bhopal, India as teaching faculty. Presently she is pursuing her PhD at Maulana Azad National Institute of Technology under the guidance of Dr. Kavita khare and Dr.S. D. Sapre. Her fields of interest are VLSI deisgn and communication.

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