Computer Aided Design Automation of an Operational Amplifier

Sandhya S. Save

***Abstract*-- The need for analog and mixed-signal design is predicted to dramatically increase over the coming years. Compared to digital designs, which can be efficiently carried out with low effort using modern high-level, logic-level, and physical-level design automation tools, analog design continues to seize a considerable portion of the total design time. Up to now, analog designers, who mostly rely on their knowledge and experience, have done most of the analog designs. It is extremely difficult for a novice designer to carry out high-performance analog and mixed-signal design. Analog design automation is also motivated by the design productivity gap considering the trend of integrating hundreds of millions of transistors on a chip, which is not feasible to rely on full-custom designed blocks. To improve the productivity and time-to-market, design automation tools are highly desirable in this area.**

A practical methodology for synthesis of analog circuits is presented in this paper. It involves embedding knowledge into pure simulation based methodology without any intervention from expert designers.

***Index Terms*—Analog circuit designs methodologies, Analog design automation, ASIC, CAD, EDA tools, Op-amps, Simulated Annealing, SPICE, SoC, Yield.**

I. Introduction

The demand for "true system integration" is leading to an increasing number of application-specific integrated circuit (ASIC) designs having nonstandard electrical and timing input/output characteristics and operating environments.

Over the past few years there has been an interest toward cheap, low power portable electronics, which is driving the semiconductor industry to move toward more and more integration of functional blocks over a single IC which is known as System-on-Chip (SoC) design. The complexity of SoC designs nowadays is ever increasing and has resulted in more integration of mixed-signal blocks over a single IC. The evolution of integrated circuit (IC) fabrication techniques is a unique fact in the history of modern industry. The improvements in terms of speed, density and cost have kept constant for more than 30 years.

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Analog and mixed-signal contents in SoCs are quickly rising. At least one forecast expects almost 70% of all IC designs to have analog or mixed-signal content by 2007[17]. A number of factors are driving this increase in analog content. The communications, consumer, and automotive markets demand more analog and mixed-signal processing than the computing market.

Due to the need to be more powerful, semiconductor manufacturers continue to innovate technologies towards smaller and smaller transistor feature sizes (for example from 0.25um to0.18um to 0.13um). As result, there is an increasing need in re-designing, functioning mixed-signal designs for new technology processes. Digital designers enjoy the use of many CAD tools that aid in the simulation, synthesis, routing, analysis, and verification of their designs, while analog designers also enjoy the use of CAD tools in areas of simulation and analysis, the area of design synthesis has yet to be completely and successfully addressed [8].

The design of active analog circuits is a difficult task due not only to the continuous nature of the signals they should process but also to the fact that all practical active devices are inherently nonlinear. Since there are no analytical methods for solving general systems of nonlinear equations, analog circuit design methodologies are based on the linearization of the devices characteristics around some operating point, limiting the set of possible solutions of a given design problem to a subset of the solutions space. Circuit synthesis is concerned with finding the topology of the circuit and its component natures and values.

Most of the performance estimation techniques are based on device models that consider physical and electrical characteristics of the circuits. Among the different models, SPICE [4] models have become the industrial standard for simulation and specification of analog circuit.

Based on device models, several techniques have been developed to evaluate the performance of analog circuits. Most evaluation approaches are either fast or accurate, but not both. These techniques can be classified as simulation-based and knowledge-based. Knowledge based Methodologies exploit domain knowledge to design analog integrated circuits and they address the design task in a full custom way. The knowledge based methodologies are mainly divided into two parts; they are the hierarchical and the fixed-topology techniques. The hierarchical design technique has been realized by OASYS [5], IDAC [6].Tools such as

DELIGHT.SPICE [3], ASTRX/OBLX [15] and AMIGO [16] have succeeded in using a flat circuit design approach with an optimization-based approach.

The design of an analog system in an analog or combined analog-digital (mixed signal) ASICs takes a considerable amount of time in comparison with a similarly complex, purely digital system. However, today about ninety percent of the total development time for mixed–signal chip is spent on designing the analog circuit and only 10 percent on the digital part [1].

The most often used analog building block is the operational amplifier (Op-amps). It is at the heart of many interface circuits, like Analog to Digital converters, Filters, etc. An efficient design of optimal Op-amp is thus a cornerstone of a design environment for many applications. Designing a good Op-amp is a rather complicated multifaceted task [9].

In this paper, the methodology used is flat circuit synthesis technique, which uses a combination of knowledge based and simulation based optimization method. This technique leads to global optimal synthesis solution. The circuit implemented is a two-stage operational amplifier with fixed topology. Simulated Annealing (SA) Algorithm implementation is used as a global optimum search engine.

II. Traditional Analog Design Flow

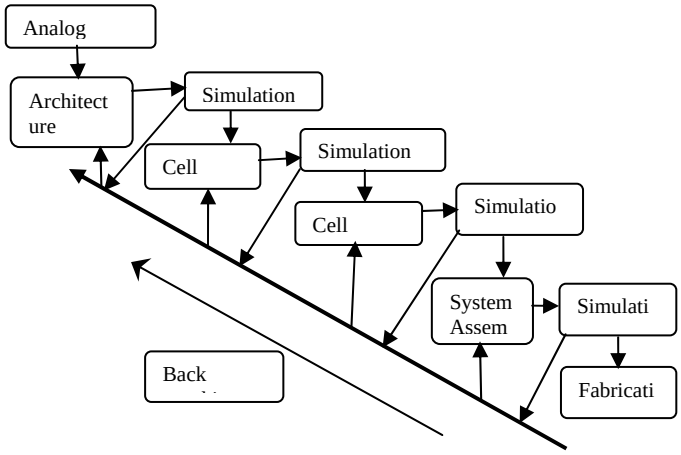

Fig. 1. Analog Design Flow

A simplified view of typical design flow is shown in Figure 1[10]. The initial stage for the design flow is an idea of an analog behavior to be implemented. The behavioral specifications are mapped into an architectural description. The simulations at this level are typically carried out using high-level models in order to validate the functionality of the concept. From these simulations, the specifications on the low-level blocks are obtained. In the next step, these cells are realized by designing the low-level building blocks that comply with the previously derived performance specification. During the layout phase the geometries for the functional blocks is determined. Finally, the building blocks are assembled to implement the desired functionality.

Throughout the design process, extensive simulations and validation steps are required. If the circuit fails to meet the specifications at some level the proceeding design steps must be revised. This may include backtracking several steps in the design process.

III. Challenges in Analog Design Flow

The traditional analog design flow, described in the previous section, suffers from several problems.

One of the most important aspects is the time spent on designing the low-level cells. The time required to design a simple amplifier could be in the order of weeks [11]. Since the large amount of chips contains both analog and digital components this poses a severe bottleneck due to the gap between analog and digital design efficiency. Decreasing the design time of analog parts in a chip will have a large impact on the time to market for the whole chip.

Another important aspect is the circuit performance. A circuit specification may contain requirements on several different performance metrics. In modern analog design, with an ever-increasing number of effects and performance metrics taken into account, the problem becomes difficult to handle. However, since most of the performance metrics are nonlinear functions of the design parameters, the probability of finding the global or even local minima is low [12]. Furthermore, due to the time involved, only a small fraction of the design space may be explored using manual design.

In order to fully explore the potential of the process technology several circuit topologies might have to be investigated [21]. Due to the cost of designing several candidate circuits this is often overlooked.

Yield is an important factor when considering the cost of a chip. Usually, manual design is carried out using nominal process parameters. When the device sizes have been determined the design is simulated using worst-case process parameters in order to stimulate process corners. Also, Monte Carlo simulations, where design and process parameters are varied according to statistical distributions, are used for this purpose [13]. Also when a simulation fails there are no ways of identifying what design parameters are causing the failure.

During the layout phase many effects that will increase the yield and ensure good circuit behavior must be taken under consideration [14]. The number of constraints on an analog layout can be large. It is therefore, hard for human designers to keep track of all these constrains and make appropriate choices when they layout the solution.

IV. Goals of Analog Design Atuomation

The designer selects an appropriate topology among various possible alternative architectures, in order to achieve higher performance for a desired application. The second step,

after the topology of the circuit and component types are fixed, consists of assigning values to the circuit parameters (e.g., widths and lengths of metal-oxide semiconductor (MOS) transistors, resistor and capacitor values, bias voltages and currents, etc.), while satisfying the desired performance criteria. Finally, the optimized circuit needs to be transformed into a layout [2]. Analog design automation can provide solutions to some of, or reduce the problems in analog circuit design and eventually reduce high-level specifications to IC masks.

The main goals of analog design automation are:

- Shortening the design time and decrease design cost.
- Increased performance
- Process technology independence
- Increase yield

V. OVERVIEW OF DESIGN METHODOLOGY

The methodology used in this paper is, a flat circuit synthesis technique, which uses a combination of knowledge based and simulation based optimization method. The embedded knowledge based Design methodology is modification of pure simulation based approach. Here, some basic knowledge about the circuit, as a set of analog design rules, is incorporated into the search mechanism. This guides the search engine towards solution in much faster times. It is also process independent and designer doesn't need to have expert knowledge about the in- depth working circuit. No complex equations and models need to be written and solved to obtain the solution. This technique leads to global optimal synthesis solution for fixed topology. Simulated Annealing (SA) Algorithm is used as a global optimum search engine.

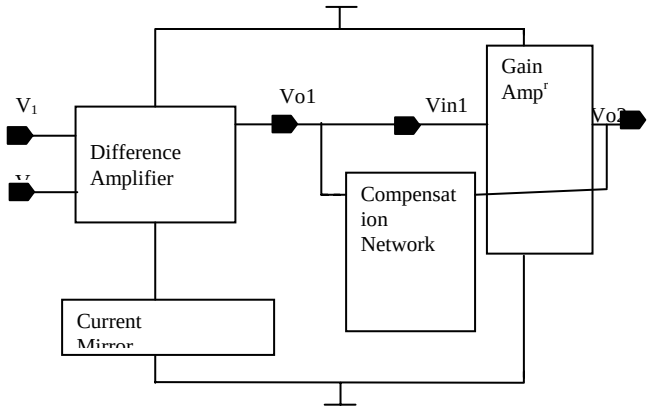

Fig. 2. Structural Partitioned Hierarchical Blocks of Op-amp

The first phase of the design methodology is hierarchical circuit partitioning and design representation in electronic format.

The second phase in the methodology is the design synthesis phase. Hierarchically partitioned sub-circuits are designed for specifications derived using a knowledge-based methodology such as circuit analysis for the sub circuit or heuristics. After sub circuits are designed, the circuit is converted into a flat circuit net list. The flat net list then simulated using an analog simulator such as SPICE [6]. The result is not near to the target specification cost of the circuit, then at least one of the sub-circuits or component redesigned with another set of design specifications for the topology.

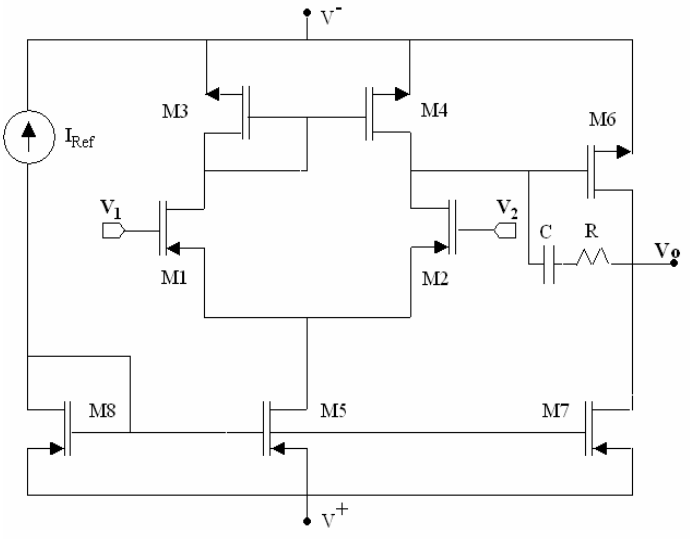

Fig. 3. Two-Stage Operational Amplifier

Phase 1: Hierarchical Circuit Partitioning

A two-stage Op-amp topology we used is shown in Fig.3. It can be partitioned into following sub circuits. A Difference Amplifier, A Gain Amplifier, A Current Mirror and Feedback network. Such a structural partitioning results in hierarchical view of the Op-amp circuit described in fig.2.

Phase 2: The Design Synthesis Phase

In this phase, hierarchically partitioned sub-circuits are designed for specifications derived using a knowledge-based methodology such as circuit analysis for the sub circuit or heuristics.

VI. SYNTHESIS RESULTS OF TWO STAGE OPERATIONAL AMPLIFIER

We synthesized the two stage Operational Amplifier using the suggested methodology. The implementation of methodology is done using standard Perl. The source code consists of about 600 lines. The code was complied on a PC with Intel Pentium processor at 2.6Ghz, (256MB RAM). Simulated Annealing (SA) Algorithm implementation is used as a global optimum search engine and the circuit simulation is done using Spice3. The models used for this simulation are level 2 for 2.0u Technology. The Values of W and L for different transistors are changed randomly during synthesis process.

The Op-amp specifications used are

- Required gain > 90db
- Gain Bandwidth Product >= 1.5MHz
- Area = Minimum

Table 4. Shows the results of Op-amp synthesis using suggested design methodology.

TABLE4 RESULTS: SYNTHESIS OF OP-AMP USING SUGGESTED METHODOLOGY

Sr No	Gain (db)	UGBP (MHz)	Bw (Hz)	Area (Sq. m) (*10-7)	Synthesis Time (Sec)	W1	W2	W3	Score
Ideal Minimum Specs	**90**	**1.5**	**35**	**10**	**600**	**0.65**	**0.35**	**0.05**	**71**
1	91.77	1.667	42.9	7.644	445	0.65	0.35	0.05	75.047
2	92.43	1.54	36.81	1.039	461	0.65	0.35	0.05	73.015
3	91.81	1.67	42.9	7.41	446	0.65	0.35	0.05	75.062
4	92.39	1.9	46.41	1.04	450	0.65	0.35	0.05	76.349
5	92.6	1.57	36.86	1.054	444	0.65	0.35	0.05	73.143
Averages					**449.2**				**74.52**

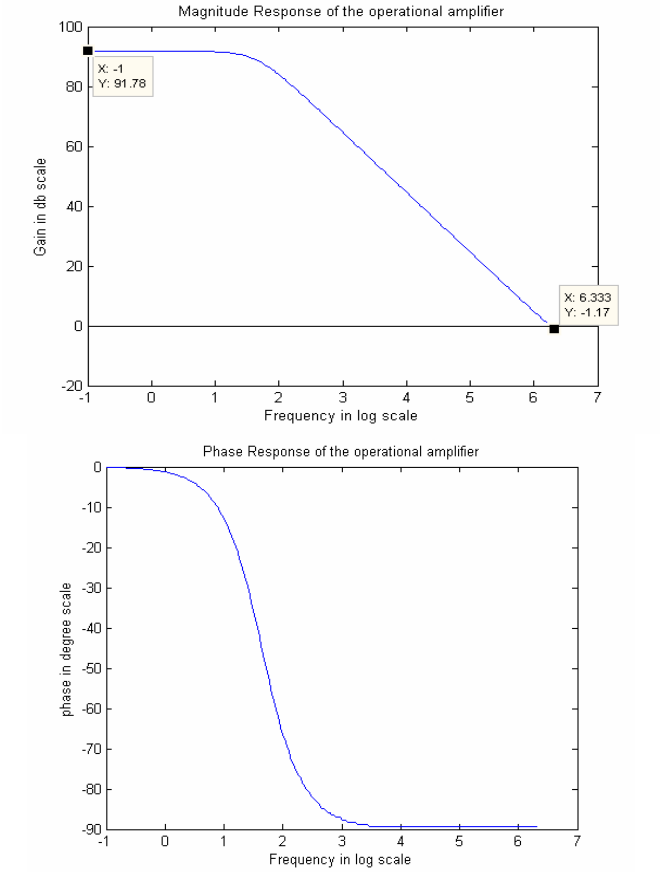

Fig5 Frequency Response of Op-amp

The following plot is plotted for one of the results listed in table 4. It is clearly seen in the graph that required gain bandwidth product is achieved with good amount of phase margin.

VII. CONCLUSION AND FUTURE SCOPE

A practical methodology for synthesis of analog circuits is presented in this paper. It involved embedded knowledge into pure simulation based methodology without any intervention from expert designers. The methodology avoids the in depth circuit analysis of large circuits and formulating design equations for large circuits. Instead, the designers have to analyze and formulate the design equations for smaller sub circuits. This is expected to save significant design time and efforts.

Experimental results show that the analog design rules in the used methodology, guide the search engine in producing constraint satisfying solution, in very short times. The synthesis tool is technology independent and can be used for synthesis of wide variety of analog circuits and topologies.

In order to accommodate other user-defined constraints, no changes in the design flow are necessary. Only the cost function is easily modified to incorporate the new constraints.

Future plan includes, to implement this methodology with more complex circuits like Analog to Digital converters (ADCs), Phase Locked Loops (PLLs), etc. and also incorporating automated topology selection from a library of components in order to make our synthesis tool complete and robust.

VIII. REFERENCES

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IX. BIOGRAPHIES

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