Low-Power VLSI Design using Dynamic-Threshold Logic

P. J. Shah, B. P. Patil, V. M. Deshmukh and P. H. Zope

Abstract :-Power dissipation is a serious concern for circuit designers. Partially-depleted SOI provides a Dynamic Threshold transistor that may be useful in reducing static power and dynamic power. DTMOS can be used to choke off leakage current and improve performance of transistors under lower voltage conditions, but suffers from high body contact resistance, Miller capacitance, area penalties, and limited operating voltage. Driving the body with a separate conditioning signal and careful design are proposed as ways to offset the above problems and still take advantage of DTMOS. A ring oscillator has been implemented to verify the use of this technology in various configurations. This information will be helpful in the design of circuits for data path elements.

The controllability of the body of the transistors allows for DTMOS circuits to be implemented. DTMOS provides both low leakage and high current drive but must be carefully used to offset decreased area and lower supply voltages. In spite of its limitations, DTMOS shows promise for power-conscious designs. When off, a DTMOS transistor chokes off leakage current and when on it enhances its current drive to offset its low operating voltage.

I. INTRODUCTION

POWER dissipation is a problem of increasing concern to designers of VLSI circuits. Figure 1 shows the estimated power dissipation trend of high-performance microprocessors through 2005 taken from the SIA roadmap [1].

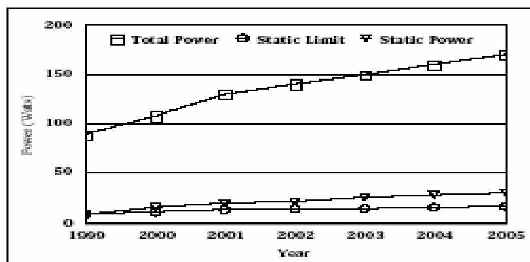

Figure 1: Projected power dissipation

Low power microprocessors follow a similar curve. Both the dynamic and static components are increasing rapidly. The power dissipation of digital VLSI systems is composed mostly of dynamic power that is derived from the equation $P_{dyn} = \alpha C_L V^2_{dd} f$, where αC_L is the effective or switching capacitance, *Vdd* is the power supply voltage, and *f* is the operating frequency.

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Since frequency is associated with improved performance, the way to reduce dynamic power is though a reduction of *Vdd* or the switching capacitance. Static power is dissipated largely in source and drain leakage currents whose magnitudes are roughly dependent on the threshold voltage, *VT*, and the sub-threshold slope of the transistors used. The higher *VT* is with respect to the voltage used to turn off the transistor, the lower the leakage current will be. Unfortunately, the drive strength of transistors depends on the relationship *Vdd-VT* so leakage currents are increasing as *Vdd* and *VT* scales to maintain drive current. The roadmap estimates that designs must eliminate 88% of the static power in low-power designs and 81% of the static power in high-performance designs by 2005 in order to return static power dissipation to an acceptable level, and suggests using multi-*VT* circuits as a solution. SOI technology provides for a dynamic-threshold transistor (DTMOS) that can be used to address both static and dynamic power dissipation by providing both low-leakage transistors and low-*Vdd* operation. The pros and cons of DTMOS and a ring-oscillator experiment designed to test DTMOS configurations will be described.

II. POWER DISSIPATION IN CMOS DIGITAL CIRCUITS

Power dissipation in CMOS digital circuits is categorized into two types: peak power and time-averaged power consumption. Peak power is a reliability issue that determines both the chip lifetime and performance. The voltage drop effects, caused by the excessive instantaneous current flowing through the resistive power network, affect the performance of a design due to the increased gate and interconnect delay. This large power consumption causes the device to overheat which reduces the reliability and lifetime of the circuit. Also noise margins are reduced, increasing the chance of chip failure due to crosstalk. The time-averaged power consumption in conventional CMOS digital circuits occurs in two forms: dynamic and static. Dynamic power dissipation occurs in the logic gates that are in the process of switching from one state to another. During this process, any internal and external capacitance associated with the gate's transistors has to be charged, thereby consuming power. Static power dissipation is associated with inactive logic gates (i.e., not currently switching from one state to another). Dynamic power is important during normal operation, especially at high operating frequencies, whereas static power is more important during standby, especially for battery-powered devices.

A. Dynamic Power Dissipation

Dynamic power primarily caused by the current flow from the charging and discharging of parasitic capacitances, consists of three components: switching power, short-circuit power, and glitching power.

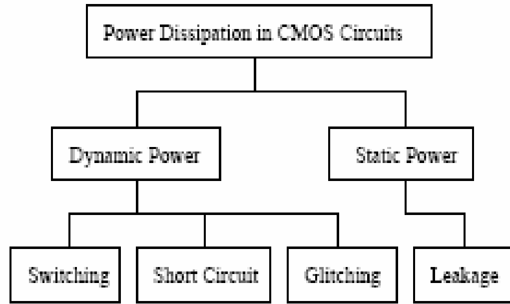

Figure 2: Different power dissipation types in CMOS circuits.

B. Static Power Dissipation

Static power is caused by leakage currents while the gates are idle; that is, no output transitions. Theoretically, CMOS gates should not be consuming any power in this mode. This is due to the fact that either pull-down or pull-up networks are turned off, thus preventing static power dissipation. In reality, however, there is always some leakage current passing through the transistors, indicating that the CMOS gates does consume a certain amount of power. Even though the static power consumption, associated with an individual logic gate is extremely small, the total effect becomes significant when tens of millions of gates are utilized in today's integrated circuits (ICs). Furthermore, as transistors shrink in size (as the industry moves from one technology to another), the level of doping has to be increased, thereby causing leakage currents to become larger. Leakage currents come from a variety of sources within the transistor. For long-channel transistors, the leakage current is dominated by the reverse diode leakage and the subthreshold leakage. Other leakage mechanisms are peculiar to the small-device geometries. In Figure 3, a summary of the leakage mechanism in a short-channel transistor is presented [5].

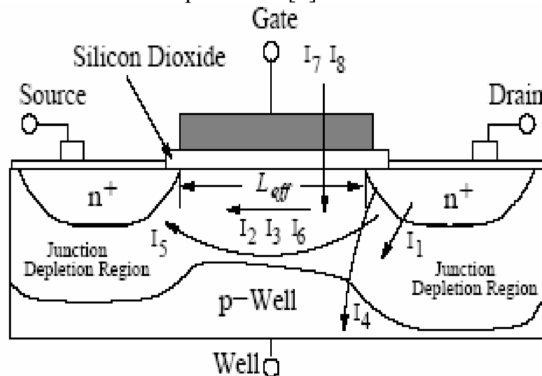

Fig.3: Leakage mechanism in short-channel nMOS transistor.

1. Reverse Diode Leakage Current (I1)
2. Subthreshold Leakage Current (I2)
3. Drain-Induced Barrier-Lowering Effect (I3)
4. Gate-Induced Drain Leakage (I4)
5. Punch-Through (I5)
6. Narrow-Channel Effects (I6)
7. Gate Oxide Tunneling (I7)
8. Hot-Carrier Injection (I8)

C. Subthreshold Leakage Reduction Techniques

Equation $P_{dyn} = \alpha C_L V^2_{dd} f$ denotes that the average switching power dissipation is proportional to the square of the power supply voltage. Therefore, the reduction of the V_{DD} significantly reduces the power consumption.

Although such a reduction is usually very effective, the inevitable design tradeoff is an increase in the circuit delay. This is obvious from the following propagation delay expressions for the CMOS inverter circuit, which are

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T,n})}\left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + ln\left(\frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1\right)\right]$$

And

$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{DD} - |V_{T,p}|)}\left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + ln\left(\frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1\right)\right]$$

The propagation delays in above equation indicate that the negative effect of reducing the power supply voltage on delay can be compensated for, if the threshold voltage of the transistor VT is reduced accordingly. However, a reduction in the VT will cause an exponential increase in the device subthreshold leakage; this increases the static power of the device to unacceptable levels. This clearly justifies the need for leakage reduction techniques, even for current technologies. Recently, an important area of research focuses on the development of circuit techniques to reduce subthreshold leakage currents that are affected by the supply voltage and the threshold voltage. The most commonly used leakage reduction techniques such as source biasing, dual VT partitioning; VTCMOS, DTMOS and MTCMOS are first reviewed. These techniques reduce leakage currents during the standby states. As technology continues to scale down, leakage currents become excessive, and therefore, need to be balanced during the active mode as well.

III. SOI

Silicon on insulator technology (SOI) refers to the use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrates in semiconductor manufacturing, especially microelectronics. SOI-based devices differ from conventional silicon-built devices in that the silicon junction is above an electrical insulator, typically silicon dioxide or (less commonly) sapphire. The choice of insulator depends largely on intended application, with sapphire being used for radiation-sensitive applications and silicon oxide preferred for improved performance and diminished short channel effects in microelectronics devices. The precise thickness of the insulating layer and topmost silicon layer also vary widely with application.

A. SOI Transistors

Various SOI device architectures (fully-depleted or FD, partially or non-fully depleted or PD) have been suggested and used for either high-speed or low power applications. Fig. 4 shows the SOI structure and its equivalent electrical structure. Depending on silicon thickness and body doping value, the channel region can be Fully or Partially depleted. Full depletion condition is reached when the total depletion charge exceeds the possible depletion charge limited by the silicon thickness. Usually, for deep submicron technologies, optimization of FD devices requires an ultra-thin silicon layer while only a thin silicon layer (100 nm) is needed for PD devices. Most of the existing, or under development, SOI technologies are based on Partially Depleted transistors.

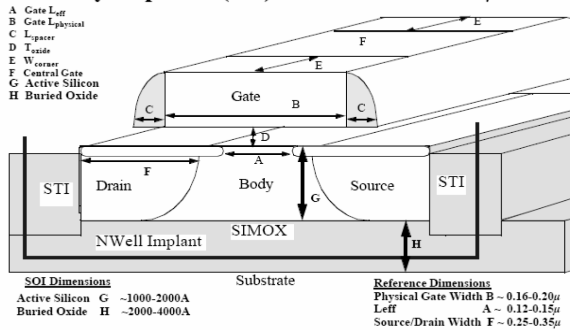

Fig: 4 Partially Depleted (PD) SOI Device

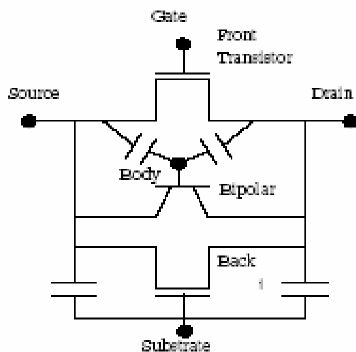

Fig. 5 Partially depleted transistors

Compared to a classical Bulk transistor, the buried oxide induces a fifth node named "Body". In the basic SOI transistor, this node is usually called "Floating Body", as it is not directly connected to a fixed potential. The electrical role of he Body of a Partially Depleted device (PD) is similar to the role of the fourth node (usually named substrate) of a bulk device. An SOI device includes firstly a front transistor with its associated impact ionization current and its diodes. Due to the Buried oxide that can act as a gate oxide, a back transistor exists. This transistor must be turned off in an optimized technology. In parallel to the MOS conduction, a bipolar device exists. Floating body effects induce positive biases on the body node, activating the parasitic bipolar transistor. Simulation of the bipolar transistor is then very important for a good SOI simulation. Finally, the low thermal conductivity of the buried oxide induces a local increase of the temperature, reducing the current level. All these phenomena induce a typical electrical behavior that requires a specific model.

B. Static behavior

In Floating Body SOI devices, the balance between impact ionization and diode current explains the well known" kink effect". The basic modeling is presented Fig. 6: As majority carriers created by impact ionization can not be evacuated in a FB device, they accumulate in the body region, leading to the forward bias of the body-to-source diode. This forward bias recombines carriers in excess in the body, until the equilibrium is reached. It reduces the device threshold voltage, creating the kink on the ID (VG) and ID (VD) curves of Partially Depleted devices [3].

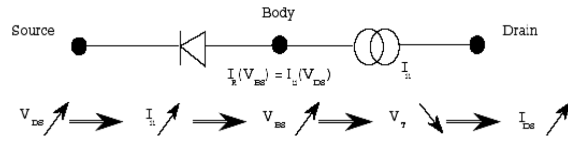

Fig. 6 Kink effect basic modeling

C. Dynamic behavior

The internal floating body is capacitively coupled to the external nodes. Its potential will then be influenced by all the variations of the other nodes [3]. Consider the transition that occurs in an NMOS in the case of an inverter that switches from one state to the other. In the OFF state, its drain is connected to VDD and its gate grounded. In the ON state, its drain is grounded and its gate connected to VDD. During the transition from OFF to ON, the space charge region goes from a small value to its maximum value. As the body is not connected to any external node, this extension of the space charge induces an excess of majority carriers that forward bias the body-to-source diode. This positive Vbody value increases the drain current during transition from OFF to ON and leads to the well-known current overshoot Fig. 7 For the reverse transition (ON to OFF), the space charge is reduced from its maximum to its minimum value, creating a lack of majority carriers. A negative Body bias occurs, leading to a current undershoot. Those dynamic effects are called "Dynamic Vt modulation", and are very interesting for Low Power applications. Indeed, during transient switching, SOI transistors are acting with an equivalent reduced threshold voltage; consequently, to get the same switching time as bulk, a lower supply voltage will be required. During switching, the body potential is determined by the initial state of the charge and by the body-to-drain/gate/source/back gate capacitive coupling. Combination of both effects leads to an history effect for the body potential and then for the associated gate delay. For each cycle, a small amount of charges is injected into the body, leading to a drift of the body voltage between two following cycles. The steady state is reached when the equilibrium between impact ionization, diodes and dynamic currents is reached.

D. SOI technology overview

The main advantage of SOI is its reduced junction capacitance due to oxide isolation of individual circuit elements, resulting in lower-power operation. Additional

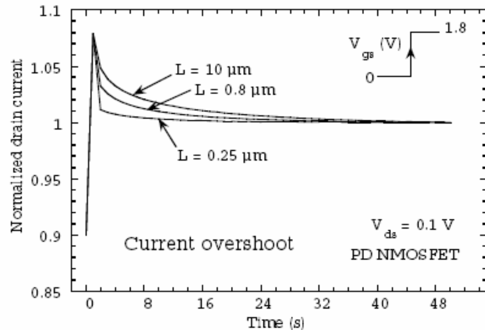

Fig. 7 Current Overshoot in Floating Body transistor

advantages are good short-channel effects due to shallow source/drain junction depth, latch up immunity, and good soft-error immunity. There are two types of SOI technology, fully-depleted (FD) and partially-depleted (PD). FDSOI fully depletes the silicon under the channel of charge carriers for the best short-channel behavior in SOI and no floating-body effects; but it suffers from high source/drain resistance and poor processing control of *VT*.

E. SOI design techniques

All major circuit families can be implemented in SOI. Leakage currents can be offset with weak keepers, level restoring transistors, or complementary pull-up networks. Floating body effects are mitigated by one or more of the following methods: pre-discharging internal nodes, alternately pre-charging and pre-discharging nodes, re-mapping logic to eliminate large soft nodes, moving parallel transistors closer to ground and re-arranging or cross-coupling inputs. A small margin may also be added to latch hold times or timing requirements may be relaxed. SOI designs can take advantage of current tool sets but there is a disadvantage in that the tools are structured around bulk design techniques, which do not leverage SOI's benefits such as increased series stacks.

IV. DTMOS STRUCTURE

SOI Dynamic Threshold MOS have been proposed for Ultra Low Power applications. A DTMOS is a Body Contacted SOI transistor who's Threshold Voltage is dynamically controlled by connecting the body to the gate. As VBS voltage is controlled, there is no floating body effect, and the threshold voltage swing is maximized, improving the Ion/off ratio. For voltages higher than 0.6V, the drain/body diode starts conducting and current limiters have to be introduced. Nevertheless, DTMOS transistors have two main drawbacks: a much larger layout area, and a larger gate capacitance [3].

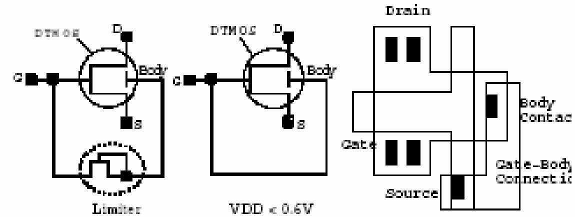

Fig: 8: schematic diagram of DTMOS

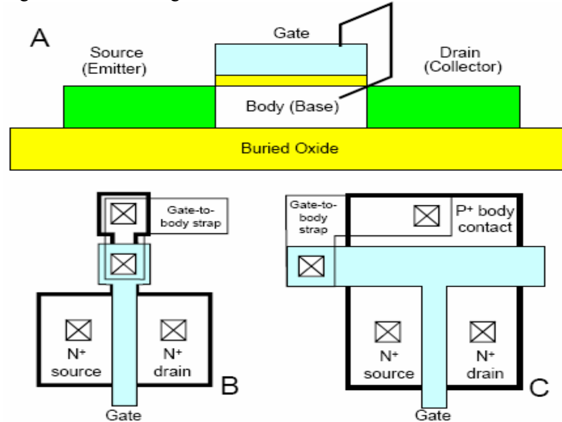

Fig 9: cross section of DTMOS

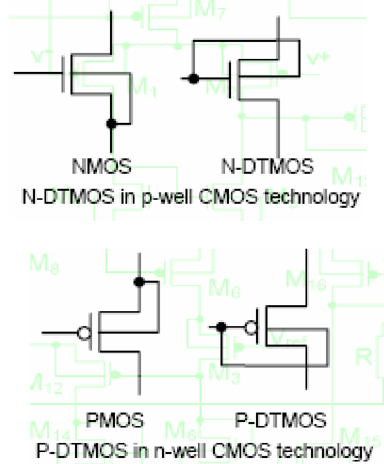

Fig: 10: Symbols of MOC and DTMOS

The DTMOS is an SOI MOSFET in which a contact is made between the gate and the body. The device was first reported in 1987 and called the" voltage-controlled bipolar-MOS device (VCBM)". Other research teams reproduced the device and named it the "hybrid bipolar-MOS device", the "hybrid-mode SOI MOSFET" or the "gate-controlled lateral BJT". These early publications placed the emphasis on the high current drive of the device due to combined presence MOS and BJT currents. Later on emphasis was put on the dependence of the threshold voltage on body potential, and thus on the gate bias, through classical body effect and the device was renamed by several teams to either the "multi-threshold CMOS (MTCMOS)", the "dynamic threshold MOS (DTMOS)", or the "varied-threshold MOS (VTMOS)". The most commonly used appellation for the device is the "DTMOS" in the USA and the "MTCMOS" in Japan [4].

An added degree of freedom in PD-SOI arises from the floating back-gate which can be controlled as an additional port. If the gate of the transistor is connected to the body, see Figure 9, a dynamic-threshold transistor (DTMOS) also called Body Controlled MOS and Variable Threshold MOS is created. Notice that as the voltage on the gate rises, the body voltage is forward-biased with respect to the source and *VT* drops. At 0 V gate input, *VT* is the same as a normal, floating-body transistor. DTMOS transistors have the advantages of low leakage current, high current drive, and little history effect while operating at low *Vdd*. There are also a number of disadvantages: the body-source and body-drain diodes limit the power supply voltage to below 0.7 V to prevent forward biasing these diodes; the high resistance of the body limits the operating frequency of the circuits; the body-drain capacitor forms a Miller capacitance that may eliminate any gain from added current drive; and the body contacts reduce integration levels.

A. Controlled body conditioning

Another problem with DTMOS is that the conditioning on the body is delayed with respect to the input and a positive body condition is not established until after switching has begun or completed. A more aggressive approach involves pre-conditioning the body to establish better switching conditions before the input arrives. For example, the third inverter in Figure 11.a has the body being driven by an inverter controlled by some external signal. It would be preferable to have the n-transistor body high before the input goes high to maximize drive current in then-transistor as it pulls down the output as in Figure 11.b. This may be referred to as positive body condition since the body voltage positively affects the drive strength of the transistor.

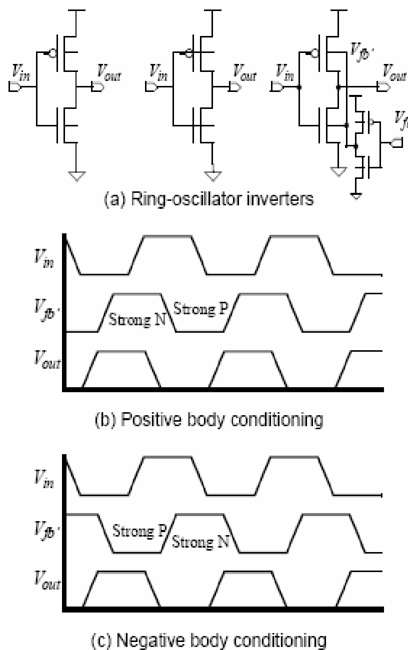

Figure 11: Ring-oscillator inverters and timing diagrams For body contacts

Figure 11. shows the opposite case, or negative body condition, where the n-transistor body is low, causing a weak transistor trying to pull down the output against a strong p-transistor. By varying the shape and position of the body bias, favorable conditions can be obtained to maximize gain and minimize leakage currents in the transistors. The ideal case would be a positive body condition only while the transistor is driving the output and a negative body condition at all other times to minimize leakage. This technique is particularly applicable to synchronous circuits where clock shaping and conditioning already takes place and phased signals are readily available. A separate clock phase, or a phase already generated, can be routed to the circuits in the data path to provide biasing in a manner that enhances the drive of transistors in the circuit while reducing leakage currents. The challenge will be in shaping that signal and aligning it for maximum benefit.

B. Ring-oscillator test chip

A ring-oscillator test macro with 17 ring-oscillators has been designed in a 0.13 μm, 8 metal layer, and 1.2V, copper PD-SOI process to compare floating-body versus DTMOS inverters and to explore the effects of body conditioning. Each oscillator is 41 stages and implements either floating body, standard DTMOS, or decoupled DTMOS as show in Figure 11.a The signal of each ring-oscillator is output on a common bus and divider. An additional bus and divider are provided to output the feed-back body-conditioning signal in the decoupled DTMOS ring-oscillators. To simulate the effect of shifting the body signal with respect to the input signal, decoupled DTMOS is implemented with the output of each inverter stage being fed forward or fed backward to drive the body of another inverter in the ring-oscillator. Figure 12 shows the implementation of feed-forward one inverter (a) and feed-back one inverter (b). Ring-oscillators implement feeding the body conditioning signal forward from one to seven inverters and backward from 0 to 7 inverters, covering a wide range of body conditions with respect to the input signal. An inverter was added to drive the body of the de-coupled oscillators to isolate the body signal from the gate and remove the extra Miller capacitance of DTMOS. This macro will allow power dissipation and frequency to be measured and compared between SOI configurations over a range of power supply voltages and body conditions. Mature circuit models for body-contacted transistors have recently become available and the ring oscillator data will help verify the validity of those models [4].

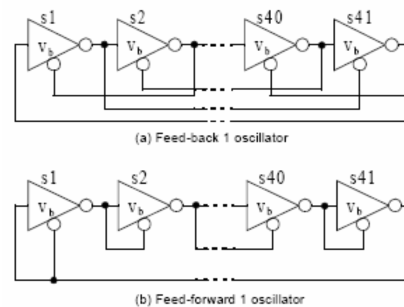

Figure 12 : Feedback and feed-forward configurations

V. CONCLUSION

SOI has become a mainstream technology used for some modern high-performance microprocessors. It is seen to be beneficial for performance and power dissipation. The controllability of the body of the transistors allows for DTMOS circuits to be implemented. DTMOS provides both low leakage and high current drive but must be carefully used to offset decreased area and lower supply voltages. In spite of its limitations, DTMOS shows promise for power-conscious designs. When off, a DTMOS transistor chokes off leakage current and when on it enhances its current drive to offset its low operating voltage. A ring-oscillator macro was developed to test the performance of DTMOS in a 0.13 μm, 8 metal, 1.1V, copper SOI process. Data from this macro will be used in developing low-power circuit styles to use for data path elements. These circuits will be tested in a multiply accumulate unit which will be built in the next phase of this research.

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VII. Biographies

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