Voltage Mode Notch Filter Using Differential Difference Current Conveyor (DDCC)

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***Abstract*--In this work a voltage mode notch filter is presented. The filter contains of two resistors and two capacitors along with a single differential difference current conveyor (DDCC). A PSPICE simulation of the proposed circuit is shown for the verification of the theoretical results.**

***Index Terms*--Notch Filter, Band stop Filter, DDCC.**

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I. Introduction

NOTCH Filters are widely used in analog signal processing to suppress the particular frequency. Current mode circuits such as current conveyors and current feed back operational amplifiers are getting much attention as compared to other active elements due to wider bandwidth, simple circuitry, low power consumptions and wider dynamic ranges. Considering these advantages of current mode circuit, several voltage – mode notch filter using various active devices have been reported [1]-[3]. However these circuits use more than one active component or several passive components. While canonical method for designing filter is also reported [2].

Because of high input impedance and arithmetic operation capability of a recently proposed active element, the differential difference amplifier (DDA) [4], the component number of circuits using DDAs can be lower than that of circuits using CCIIs. Therefore, the advantages of CCIIs and DDAs are combined and extended to two new and similar versatile building blocks, called the differential voltage current conveyor (DVCC) [5]. Some application of it using these two elements has been presented in the literature [7]

In this work, we propose a single DDCC based canonical voltage mode notch filter employing two resistors and two capacitors.

II. PROPOSED CIRCUIT

The DDCC, whose electrical symbol is shown in Fig. 1, is five terminal devices whose characteristics are described by

$$\begin{bmatrix} I_{y1} \\ I_{y2} \\ I_{y3} \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_{y1} \\ V_{y2} \\ V_{y3} \\ I_x \\ I_z \end{bmatrix} \quad (1)$$

where the plus and minus signs indicate whether the conveyor is configured as a plus or minus type circuit, termed DDCC+ or DDCC- , respectively.

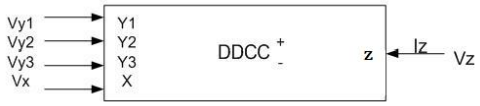

Fig.1 Electrical Symbol of DDCC

Using one DDCC+, voltage mode notch filter that contains two resistors and two capacitors are implemented. The impedances Z1 (resistance R1 in series with capacitor C1), Z2 (resistance R2 in parallel with capacitor C2) along with DDCC is shown in the Fig. 2.

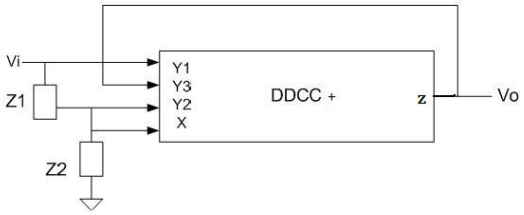

Fig. 2 Proposed canonical voltage mode notch filter

Nodal analysis yields the following transfer function:

$$\frac{V_0}{V_i} = \frac{s^2 + s\left(\frac{1}{R_1C_1} + \frac{1}{R_2C_2} - \frac{1}{R_1C_2}\right) + \frac{1}{R_1R_2C_1C_2}}{s^2 + s\left(\frac{1}{R_1C_1} + \frac{1}{R_2C_2} + \frac{1}{R_1C_2}\right) + \frac{1}{R_1R_2C_1C_2}} \quad (2)$$

The above transfer function shows the presented filter is band stop filter. The notch filter is a unique case of it when the zeros of the transfer function are complex conjugate at the imaginary axis. By considering $R_2=2R_1$ and $C_1=2C_2$ we get

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$$\frac{V_0}{V_i} = \frac{s^2 + \frac{1}{4R_1^2C_2^2}}{s^2 + s\frac{2}{R_1C_2} + \frac{1}{4R_1^2C_2^2}} \quad (3)$$

which is the transfer function of the notch filter. The central frequency of the notch filter is

$$\omega_0 = \frac{1}{2R_1C_2} \quad (4)$$

The pole sensitivities of the proposed circuit as notch filter are given as

$$S_{R_1}^{\omega_0} = S_{C_2}^{\omega_0} = -1$$

Which are no more than unity in magnitude.

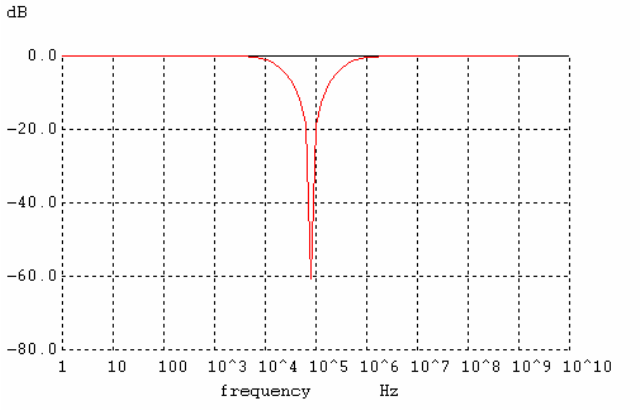

Fig. 3 Magnitude Response of notch Filter

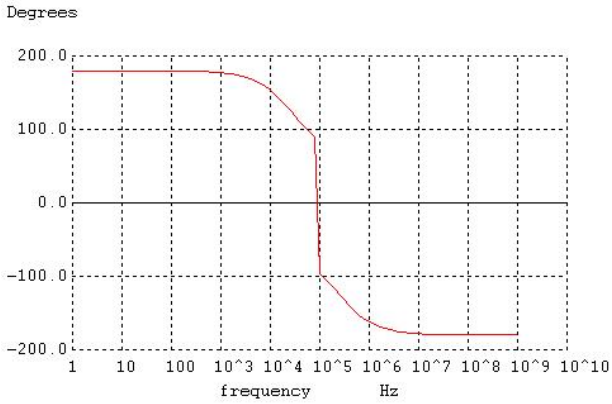

Fig. 4 Phase Response of notch Filter

III. NONIDEALITY ANALYSIS OF DDCC

Taking into consideration the DDCC+ non idealities the port relations in (1) can be expressed as

$$V_x = \beta_1 V_{y1} - \beta_2 V_{y2} + \beta_3 V_{y3} \;\&\; I_z = \alpha I_x \quad (5)$$

Reanalysis of the filter circuit yields the following modified transfer function:

$$\frac{V_0}{V_i} = \frac{1}{\beta_3} \times \frac{sR_2C_2(1+\beta_2-\beta_1) - \beta_1(1+sR_1C_1)(1+sR_2C_2)}{s^2R_1R_2C_1C_2 + s(R_1C_1 + R_2C_2 + R_2C_1) + 1} \quad (6)$$

From the transfer function it is clear that central frequency ω_0 is independent from the nonidealities .

$$S_{\beta_1,\beta_2,\beta_3}^{\omega_0} = 0 \quad (7)$$

IV. SIMULATION RESULT

The proposed circuit was simulated using PSPICE. The DDCC was realized by the CMOS implementation in Fig. 5[8] using 0.5µ m MIETEC CMOS technology process parameters. The supply voltages were taken as VDD = 2.5V and VSS = -2.5 V. The biasing voltage VBB was taken as -1.7V. The aspect ratios of the MOS transistor are given in Table 1. The DDCC based circuit of fig. 2 was designed with $R_2 = 2\ R_1 = R = 2K\Omega$ and $C_1 = 2\ C_2 = C = 1nF$. The designed pole frequency (ω_0) was 50 KHz. The simulation result is shown in Fig.3 and Fig 4.

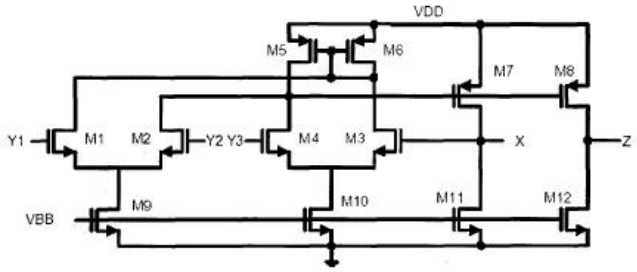

Fig 5: CMOS realization of DDCC

TABLE 1:
TRANSISTOR DIMENSIONS OF CMOS DDCC+ CIRCUIT

Transistor	W(µm)	L(µm)
M1-M4	0.8	0.5
M5-M6	14.4	0.5
M7-M8	4	0.5
M9-M10	10	0.5
M11-M12	45	0.5

V. CONCLUSION

In this work, a voltage mode notch filter using DDCC is proposed. The proposed circuit contains a single DDCC, two capacitors and two resistors with a good attenuation at the central frequency. Non ideal analysis was carried out. Sensitivity to the parameter variation, which is calculated, is not more than 1. PSPICE simulation results verify the theoretical results. The proposed notch filter has been simulated using Spice program to verify the theoretical analysis. To implement the DDCC+ the CMOS model is taken for the paper [6]. The value of R and C are 1KΩ and 1nF respectively. The obtained the notch frequency is 1.59e+05 Hz.

VI. REFERENCES

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