Analysis and Comparison of Subthreshold 1-Bit Full Adder Cells

Naushad Alam, Kureshi A. K. and Mohd. Hasan

***Abstract*- This paper presents performance analysis and evaluation of the main topologies of 1-bit full adder cells operating in sub-threshold region. Seven full adder cells were chosen from the literature, including the most interesting of those recently proposed, and are compared with respect to delay, power consumption, driving capability and Power-Delay-Product (PDP). Both the conventional structure and dynamic threshold voltage MOS (DTMOS) structure of all the selected full adder cells have been investigated for varying load, with simulation runs on HSPICE for 65nm technology using Berkeley Predictive Technology Model (BPTM). The simulation results show that the standard CMOS structure is most efficient and a marginal performance improvement can be achieved with DTMOS structure.**

***Index Terms*— DTMOS, Full adder, Sub-threshold, Ultra-low Power, VLSI.**

I. Introduction

ADDITION is one of the most fundamental arithmetic operations. It is used extensively in many VLSI systems such as application specific DSP architectures and microprocessors. In addition to its main task of adding two binary numbers, it is the nucleus of many other useful operations such as subtraction, multiplication, division, address calculation, etc. Hence, optimization of the adder both in terms of power and speed should be pursued.

Digital subthreshold circuits are currently used for some low power applications such as wristwatches, hearing aids, pacemakers and wireless communication systems [1]. In sub-threshold circuit design, supply voltage must be scaled down below the threshold voltage. This ensures that the transistor channel is never fully inverted and the load capacitance is charged or discharged by the sub-threshold leakage current. The low level of supply voltage satisfies the ultra-low power requirement with acceptable performance. When adder circuits operate in sub-threshold region, they have different characteristics than those of the adders working in the super threshold region.

Until now, in the literature there have been some comparisons between full adder circuits operating in sub-threshold region [2], [3]. However, issues of increased sensitivity to temperature & process variations and the use of DTMOS [4] structure have not been addressed. In this paper, two structures, conventional and DTMOS, of seven full adder cells are characterized and evaluated for delay, power consumption, driving capability, PDP, and sensitivity to temperature & process variations in sub-threshold region. The analysis and comparison developed here for full adder cells operating at a frequency of 100 KHz with V_{dd}=0.25V have been carried out with simulation runs on HSPICE for 65nm technology node using Berkeley Predictive Technology Model (BPTM) [5]. The rest of the paper is organized as follows. Section 2, briefly describes the structures of selected full adder cells. Analysis and comparison is developed in Section 3. Improved characteristics with DTMOS structure is reported in Section 4. Summary and conclusion are given in Section 5.

II. The 1-Bit Full Adder Cells

The full-adder function can be described as follows: Given the three inputs A, B, and C_{in}, it is desired to calculate the two outputs *sum* and C_{out}, where

$$Sum = A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = A.B + C_{in}.(A \oplus B) \quad (2)$$

The following are the standard implementations of the full-adder cell which are analyzed and compared in this paper:

1) The CMOS full adder [6] has 28 transistors and is a simple implementation of equations (1)-(2) with the CMOS structure.
2) The Mirror adder [7] is simply derived from CMOS adder by directly connecting the series PMOS transistors to the supply. It also uses 28 transistors.
3) The CPL full adder [7] has 32 transistors and is made up of NMOS pass-transistor and has differential inputs and outputs. Cross-coupled PMOS transistors are introduced to achieve level restoration.
4) The TG full adder [8] is based on transmission gates and introduced for its low power dissipation. It has only 16 transistors.

Naushad Alam is with the University Polytechnic, Aligarh Muslim University., Aligarh-202002, India. (phone: +919897165051; e-mail: itsnaushad@rediffmail.com).

A. K. Kureshi is pursuing Ph.D. in the Electronics Engineering Department, Aligarh Muslim University, Aligarh-202002 INDIA (e-mail: akkureshi@rediffmail.com).

Mohd. Hasan is with the Electronics Engineering Department, Aligarh Muslim University, Aligarh-202002 INDIA (e-mail: m_hasan786@rediffmail.com).

5) TGdrivcap (TG full adder with driving capability) full adder [8] has 26 transistors and solves the poor driving capability of TG full adder.
6) The HPSC (hybrid pass logic with static CMOS output drive) full adder [9] implementation has 22 transistors and uses hybrid-CMOS logic design style.
7) The hybrid-CMOS full adder [10] uses 24 transistors to implement equations (1)-(2).

III. Analysis of the Full Adder Cells

All the full adder cells are analyzed with V_{dd} = 0.25V for an input frequency of 100 KHz. Structures were simulated with different load capacitances ranging from 100fF to 500fF to evaluate the driving capability. An inverter has been added before all the inputs to make the test more realistic. Table I shows the simulation results at 50^0C and C_{Load} = 200fF.

It is clear, from results that the robust structures of CMOS and MIRROR cells perform well in most aspects, having lowest delay and PDP with second lowest power dissipation. Also, they are most suitable in configurations with high fan-out, as their performance is least degraded with varying load.

The CPL is not useful for ultra-low power applications as it dissipates maximum power due to its high transistor count, high switching activity of intermediate nodes and overloading of its inputs. Even though, it has delay comparable to CMOS and MIRROR cells but the PDP is maximum.

The TG full adder has lowest transistor count, as well as few internal switching nodes, resulting in the lowest power dissipation of all analyzed full adders. However, the delay is maximum because of its coupled structure [11]. The inputs are coupled to the output and thus the delay heavily depends upon the load capacitance, shown in Fig.3. It makes it unfeasible for deep sub-threshold operation, as well as in configurations with high fan-out.

The TGdrivcap has better performance than TG circuit by introducing inverters to decouple inputs from output, which ultimately increases the driving capability of the circuit. The low power dissipation combined with comparable delay gives this cell better PDP than CPL full adder.

The HPSC and hybrid-CMOS full adders, using hybrid logic style, have power consumption comparable to standard CMOS adder attributed to their lower transistor count and lesser internal switching nodes. The delay is large because of the use of transmission gates. Moreover, the modules chosen were optimized [9], [10] for super-threshold operation, and, hence for sub-threshold operation hybrid logic style full adders should be redesigned and optimized.

Increased sensitivity to temperature and process variations is a major issue in sub-threshold region. The effect of temperature variations is analyzed by simulating the structures from 25^0C to 125^0C at 100 KHz with V_{dd} = 0.25V. The effect of process variations is analyzed by varying the threshold voltage (V_{th}) of both NMOS and PMOS transistors by 5% in both the directions from their original designed values.

TABLE I
SIMULATION RESULTS FOR STANDARD STRUCTURES

Full Adder	Trans. Count	Power ($x10^{-9}$ W)	Delay ($x\ 10^{-9}$ S)	PDP ($x\ 10^{-18}$ J)
CMOS	28	5.376	55.361	297.615
MIRROR	28	5.41	55.374	299.573
CPL	32	12.455	57.097	711.143
TG	16	4.154	183.01	760.233
TGdrivcap	26	7.156	59.793	427.879
HPSC	22	5.483	126.31	692.558
Hybrid-CMOS	24	5.213	129.13	673.155

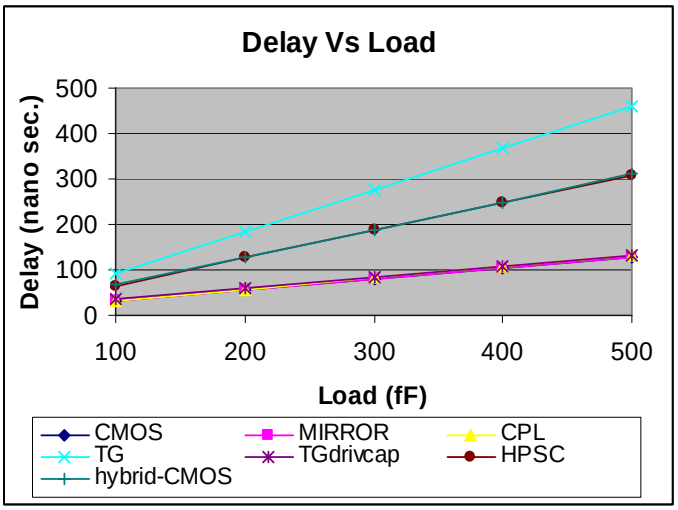


Fig. 3. Delay with varying load capacitance

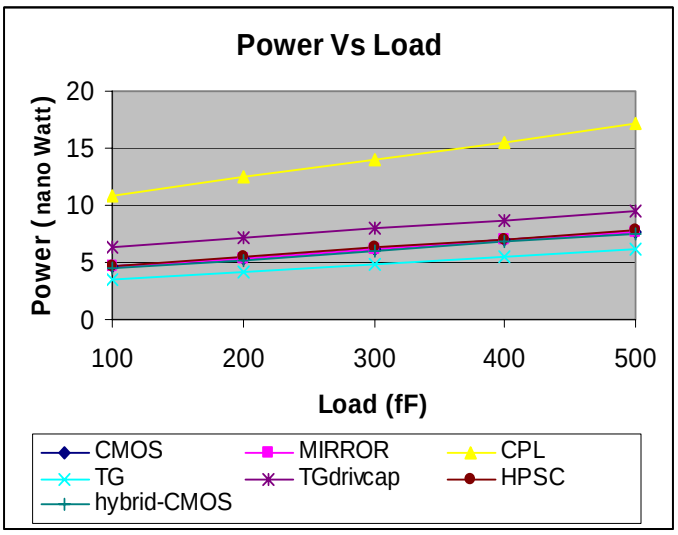


Fig. 4. Power dissipation with varying load capacitance

We use the "Delvto" option of HSPICE to change V_{th} as suggested in [12]. Fig.6 and Fig.7 compare the variations in delay by varying the temperature of operation and the threshold voltage of the transistors respectively. CMOS, MIRROR, CPL and TGdrivcap full adders are least sensitive to these changes and maintain more stable operation.

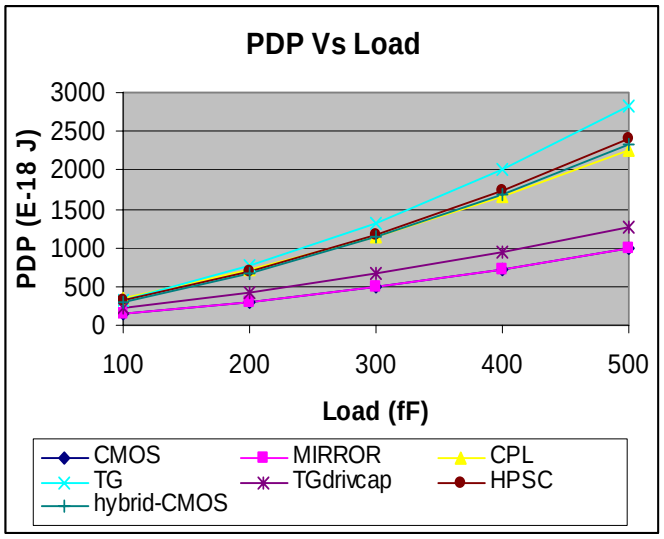


Fig. 5. Power-Delay-Product with varying load capacitance

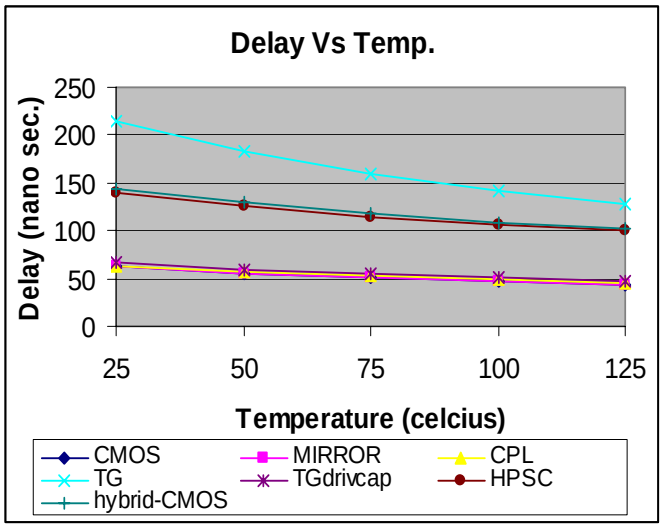


Fig. 6. Delay with varying Temperature

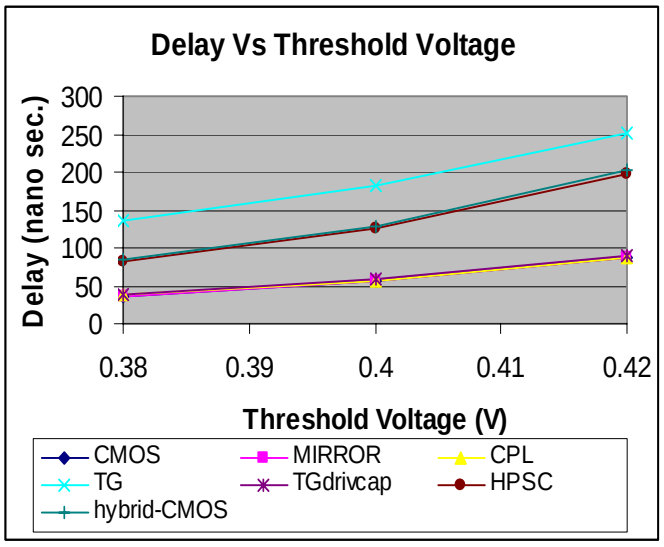


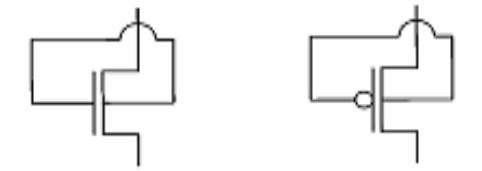
Fig. 7. Delay with varying threshold voltage (V_{th})

IV. DTMOS Full Adder Cells

The DTMOS full adder is implemented with transistors whose substrate and gate are tied together, as shown in Fig. 8. The higher on current of DTMOS logic causes it to have higher power consumption, but can switch much faster than regular MOS logic. Although DTMOS gate capacitance is larger than that of standard MOS gate capacitance, but the increase in current drive of DTMOS outweigh the increase in its gate capacitance.

One of the roadblocks in sub-threshold operation is the increased sensitivity to temperature and process variations. In [4], it has been shown that the sensitivities of conventional MOS logic circuits can be reduced using DTMOS structure. All the full adder cells were redesigned with DTMOS and analyzed for their characteristic parameters. The results with V_{dd}=0.25V, C_{Load} = 200fF and 100 KHz input frequency at 50^0C are reported in Table II.

The results show that the delay of DTMOS full adder structures has reduced by more than 50% (due to marginal increase in ON current and hence drive capability) with less than 10% increase in power dissipation. For all the full adders' delay and PDP is lower for corresponding DTMOS structure and, therefore, is more energy efficient. The delay of three selected full adder cells, both standard and DTMOS structures, versus the temperature is plotted in Fig. 9 and Fig.10 shows the delay variations with change in threshold voltage. It is clear that the later structure maintains more stable operation over a range of temperature and process variations.



DTNMOS DTPMOS

Fig. 8 Dynamic Threshold MOS transistor

TABLE II
SIMULATION RESULTS FOR DTMOS STRUCTURES

Full Adder	Trans. Count	Power (x 10^{-9} W)	Delay (x 10^{-9} S)	PDP (x 10^{-18} J)
CMOS	28	5.850	26.650	155.90
MIRROR	28	5.883	26.659	156.83
CPL	32	12.878	26.550	341.91
TG	16	4.352	64.251	279.62
TGdrivcap	26	7.464	27.938	208.53
HPSC	22	5.797	53.656	311.04
Hybrid-CMOS	24	5.485	55.910	306.67

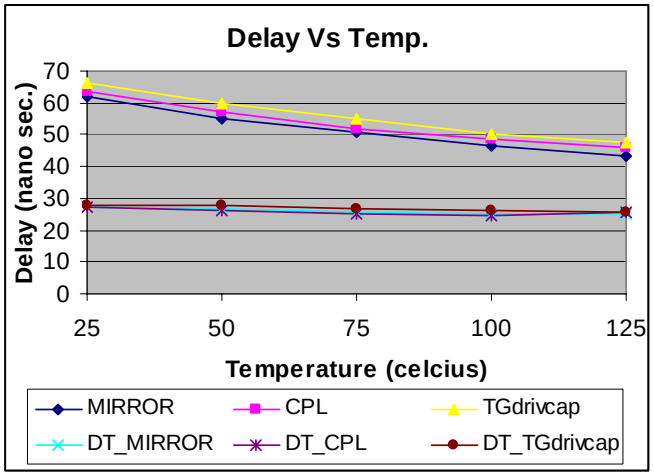


Fig. 9. Delay with varying Temperature

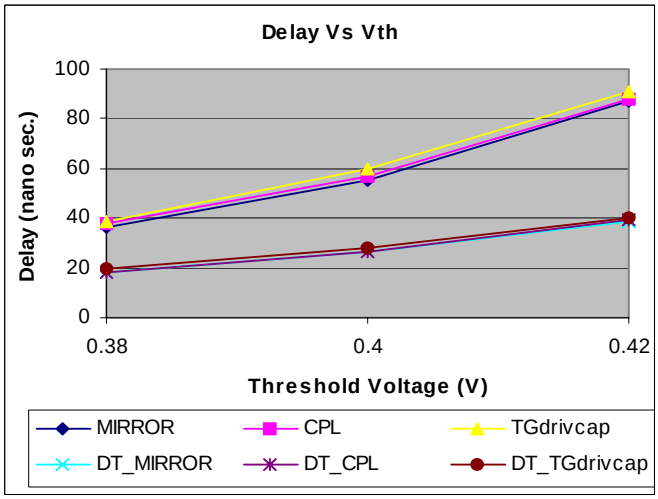


Fig. 10. Delay with varying threshold voltage (V_{th})

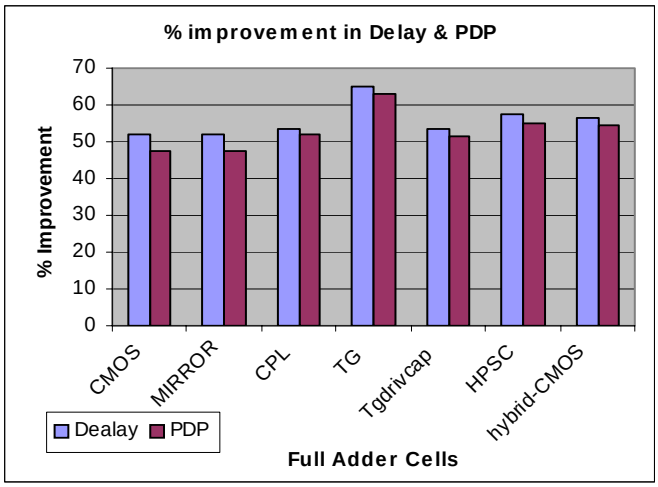


Fig. 11. Improvement in Delay & PDP with DTMOS

V. Summary and Conclusion

In this work, conventional and DTMOS structure of seven full adder cells were analyzed in sub-threshold region for ultra low power operation. First, the conventional structures were analyzed and compared for various characteristic parameters and it has been found that the CMOS structure is best from delay and PDP point of view whereas power is minimum for TG full adder. MIRROR adder closely follows CMOS cell and offers almost equal performance. Later, the DTMOS full adders were simulated and analyzed for the same simulation setup. Observations show that DTMOS full adder cells have superior robustness and tolerance to temperature and process variations besides having smaller delay and PDP.

The results from Section 2 and Section 3 show a marginal improvement in the characteristic parameters of all the full adder structures with DTMOS. Fig. 11 plots the percentage improvement in delay and PDP with DTMOS structure. TG full adder shows maximum improvement as it is most affected by parameter variations.

This paper concludes that CMOS structure is best suited for sub-threshold operation and marginal improvement can be achieved with DTMOS structure. However, DTMOS can only be implemented in triple well process technology whereas it can be easily implemented in SOI technology where the body of each transistor is inherently isolated. The additional increase in area and process complexities can be compensated by its higher operating frequency, and driving capability while maintaining lower PDP.

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VII. BIOGRAPHIES

Naushad Alam received his B.Tech. degree in Electronics & Communication Engineering in 2003 from Jamia Millia Islamia, New Delhi. He joined as lecturer in Electronics Engineering, University Polytechnic, A.M.U., Aligarh in 2003. Presently he is pursuing M.Tech. in the Electronics Engg. Department, A.M.U. His research interests include Low Power VLSI design, Subthreshold Logic for ultra-low power applications, Network on Chip etc.

Kureshi A. K. was born in Ahmendnagar on June 9, 1971. He graduated and post-graduated in electronics engineering from the Pune University. He worked as Asstt. Professor at PDVVP. College of Engineering Ahmednagar. Presently he is pursuing PhD in the department of electronics engineering, Aligarh Muslim University Aligarh. His special field of interest includes low power high speed FPGA design.

Mohd. Hasan received the B.Sc. degree in Electronics Engineering in 1990 from A.M.U.,Aligarh. Subsequently, he completed his M.Tech. in Integrated Electronics & Circuits from Indian Institute of Technology, Delhi. He joined as lecturer in the Electronics Engg. Department, A.M.U. in 1992. He became a reader in 1997. He has completed his PhD. in Low Power Architecture for Signal Processing and Telecommunications in the School of Engineering and Electronics, University of Edinburgh, U.K., in 2004. His research interests include low power IC design for wireless communications, and configurable systems on FPGA and so on.