Review of Radiation Hardness Capabilities of SOI Based SRAM

S. S. Rathod, *Member, IEEE*, S. Dasgupta, *Member, IEEE* and A. K. Saxena, *Senior Member, IEEE*

Abstract—**This paper presents a literature survey of radiation hardness capabilities of silicon on insulator (SOI) based static random access memory cell (SRAM). Various options at the process as well as device level for the reduction of soft error rate are reviewed. Issues related to critical parameters for SOI based SRAM design, front vs back exposure, effect on SER due to process variations, multi bit upsets, simulation and modeling of SER are discussed. Possibilities for further improvement are highlighted in the paper.**

***Index Terms*-- MOSFET, SRAM, SOI, Single Event Upset, Soft Error Rate, Radiation Effects.**

I. Introduction

UNSEEN, but all around us, are microscopic ionizing radiation sources. The interaction of cosmic rays and particles, for example from solar flares, with atoms in our atmosphere produces showers of neutrons and protons. When these particles penetrate electronic devices (even at ground level), they can result in spurious currents that corrupt information or even permanent damage. Energetic particles emitted from packaging materials and over layers also contribute to the problem. Technology scaling to and below nanometer dimensions, and to low voltages, means that very small amounts of charge and low current levels are associated with information signals inside of integrated circuits.

The complexity of the interaction of terrestrial radiation with the materials used to make circuits and the technology and design (layout) dependence of the resulting effects, make analysis and mitigation extremely challenging. Recently, the desire to use advanced commercial technologies in space applications has resulted in direct study of some of the most advanced and emerging semiconductor technologies [1]. This has also facilitated the ongoing development of an infrastructure to analyze single event effects, calculate damage and error rates, and optimize technologies and designs. These capabilities are now being applied to commercial technologies and applications, as well as being used to explore the effects in emerging technologies. Intel has stated that single event effects manifested as soft errors are the second greatest reliability concern after gate leakage currents. At the recent IEEE Radiation Effects Conference, IBM presented results indicating that even advanced SOI CMOS devices are now sensitive to extremely low levels of injected charge.

An important advantage of SOI is having superior radiation hardness capabilities due to the presence of buried oxide [1]. Scaling has drastically reduced both good and bad on-chip capacitances, leaving even the logic on recent generation hardware vulnerable to radiation-induced soft errors. SOI helps to address this concern, which otherwise discourages the application of VLSI CMOS in satellite and aerospace platforms. SOI technology has long been popular in extraterrestrial electronics applications due to its increased immunity to radiation-induced logic errors. In addition, even in earthbound applications, the fail rate due to alpha and cosmic radiation has been steadily increasing as scaling reduces the capacitances on each node. Soft error upsets decrease the field reliability of a product. But like defect-related field fails, they are a fact of life for our industry. The good news is that their occurrence rate can be predicted, and the composite reliability of a total system can be budgeted to accommodate these exposures.

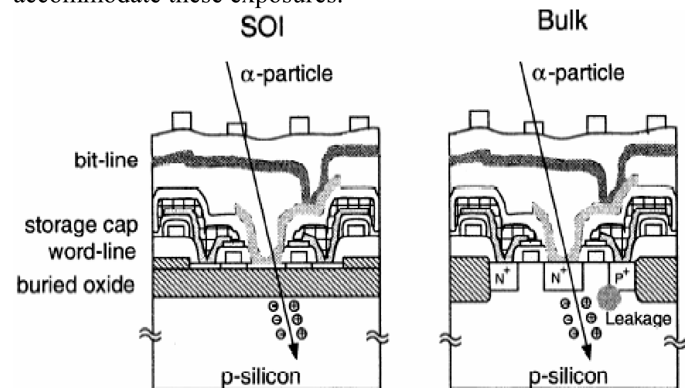

Fig. 1. SOI Device Structure of MOSFET at 1micron (Adapted from Kuo *et. al.* [1])

When high-energy particles pass trough a silicon wafer, a large quantity of electron-hole pairs are generated in the substrate as shown in Fig. 1. For the bulk CMOS devices, these electron-hole pairs may be absorbed by the source/drain to produce a large leakage current, which may affect the operation of the related circuits [1]. It may trigger latchup to

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cause breakdown of the circuit. For SOI devices, due to the separation of the device from the substrate provided by the buried oxide, the above drawbacks of the bulk devices do not appear. Thus, the soft error immunity of the SOI devices is better [1]. Comparison of soft error rate of Bulk CMOS and SOI is shown in Fig. 2.

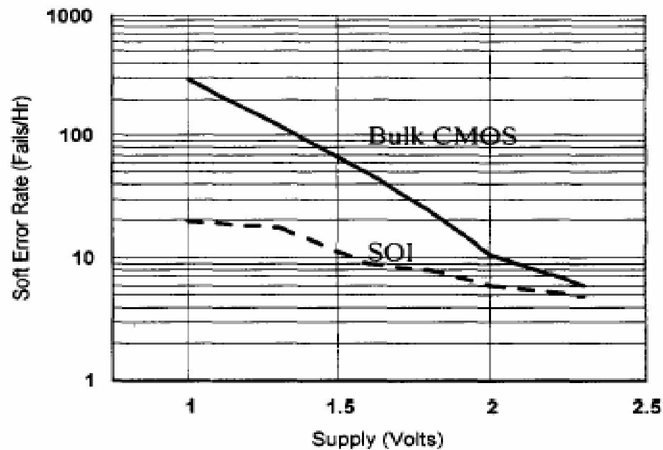

Fig. 2. Soft Error Rate for Bulk CMOS and SOI when placed under active alpha particle radiation source (Adapted from Kuo *et. al.* [1]).

A bit error is called a soft-error *if the data is corrupted but the device itself is not damaged.* In contrast, a permanent device failure is called a hard error [2]. *Soft errors refer to false data states* induced in the microprocessor logic or memory by the instantaneous introduction of high amounts of unexpected charge, created by a radiation event [3]. Charge can be created as a result of incident alpha particles or high energy protons or neutrons (cosmic rays). The SOI MOSFET's response to soft error events is a balance of a number of compensating effects. Soft Error Rate is the fail rate of an array due to alpha and cosmic radiation, commonly measured in fails per thousand hours per thousand bits.

The vulnerability of the static 6-device SRAM cell to alpha and cosmic radiation incidence events has become profound with continued process scaling. Once only a concern in the DRAM domain [1], the reduction in capacitances with successively improving lithography generations has raised the SER concern in SRAM memory and in selected logic topologies as well. If not addressed through other means, higher reliability requirements often force the SRAM designer to increase SRAM storage cell size by using non-minimum layout dimensions. SOI's superior innate resilience to incident alpha particles and cosmic rays again makes this technology timely. Recent experiments [3] on commercial Bulk and partially depleted SOI state that both technologies are equally sensitive to neutron SER from the 180-nm node. Moreover, a trend of SER saturation or reduction on a per-bit basis is reported for SOI and Bulk technologies. This behavior is observed for SER from both neutrons and alpha particles sources.

Owing to the small soft error rate SOI technology is suitable to integrate low voltage SRAM [4]. Soft error upset immunity in SRAM, which has been steadily eroding from generation to generation in bulk CMOS, improves in SOI in a given lithography generation, as a result of a number of balancing mechanisms. While SOI soft error immunity erodes with lower voltage, it does so at a much slower rate than bulk [5]. SOI has been said to love lower voltages: this observation [6] is most readily apparent in the behavior of on-chip SRAM cache.

The amount of charge generated in SOI is strongly dependent upon a number of factors, all of which have a probability distribution associated with them. These include *the energy of the incident particle, the vertical angle of incidence with respect to the surface, the horizontal angle of incidence with respect to the device orientation, the channel length of the device, the location of incidence with respect to the device, and the local impurity concentration* [7].

II. CONTRIBUTION OF ALPHA AND NEUTRON PARTICLES

Alpha particles are emitted by radioactive impurities that are present in the IC package and in the IC itself while Cosmic neutrons originate from the interaction of high-energy cosmic rays with atoms in the earth's atmosphere [2]. An alpha-particle is capable of ionising silicon by generating electron–hole pairs. Neutrons do not directly produce charges in silicon, but can interact with silicon atoms. The products of this interaction then ionise the material. When an ionising particle, e.g., an alpha-particle, intersects a reverse-biased pn-junction, this junction can collect the charges that are generated along the particle track. Both drift, in the disturbed electric fields, and diffusion play a role in the collection of charge carriers.

In SOI MOSFETs the bipolar effect occurs when α-particle hits a channel region. Typically as shown in Fig. 8, α - particle-induced bipolar current flows over a long period [8]. Therefore, it is important to clarify the effect of the bipolar current, the difference in noise currents of SOI and bulk MOSFETs, in SOI SRAM. Tosaka *et. al.* [8] found that the α-particle-induced generated charge Q_{oc} determines the soft error in SOI SRAM and showed that the SER in submicron SOI SRAM without body contacts is sometimes larger than that for bulk SRAM due to bipolar effect as shown in Fig. 9. This suggests the necessity for body contacts or for other technologies in SOI SRAM structure to reduce the bipolar effect [8].

III. VARIOUS METHODS FOR REDUCTION OF SER

Following are the various published methods reviewed for the reduction of SER.

A. *Body-Fixed Scheme*

Brady *et. al.* [9] [10] in 1998 reported that fully depleted SOI requires no body ties for SEU hardening. Yoshiki *et. al.* [11] described 128Kb synchronous SRAM with body-fixed structure and compared with those of 128Kb SRAM with floating body configuration. Fig. 3 shows SOI MOS structure

with and without body ties. The body regions are fixed to the supply voltage or ground voltage to suppress the parasitic bipolar action. The alpha-particle induced soft error rate of the body-fixed SRAM was considerably lower than that of the floating-body SRAM. The ratio of the soft error rate is about 1/300. In bulk-CMOS devices, soft errors are mainly caused by the funneling effect due to alpha particle hits to the drain region. As shown in Fig. 5 the measured soft error rates [11] show that the body-fixed structure is effective to suppress soft errors caused by parasitic bipolar effect.

Due to the field-shield gate, LOCOS has been used [1] to isolate the NMOS device from the PMOS device using the body-fixed scheme such that latchup can be avoided. In contrast, for the SOI SRAM with the body-floating scheme, N+ and P+ drain regions have been used to isolate the PMOS device from the NMOS device in order to inhibit latchup. Therefore, the layout area is smaller using the body-floating scheme. By using the body-fixed scheme in the SOI SRAM, its soft error rate is reduced owing to the inhibited parasitic bipolar device. However, the memory cell occupies a larger layout area [1]. K. Hirose *et. al.* [12] as shown in Fig. 4 revealed an increase in the threshold LET (Linear Energy Transfer) from 5.8 to 8.1 MeV/(mg/cm2) that was mostly due to the reduced bipolar gain of the parasitic bipolar transistor and partly due to the added capacitance, which were both related to the body-ties.

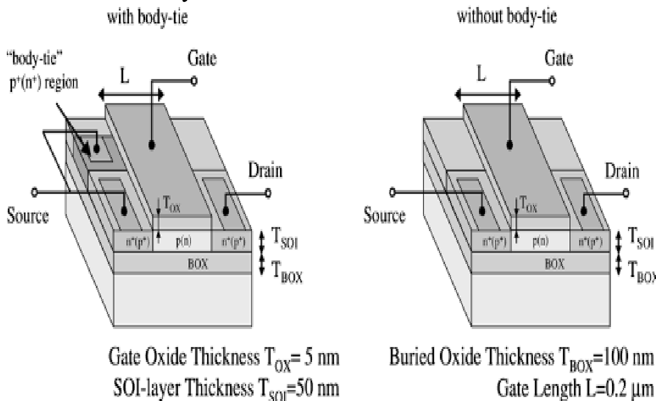

Fig. 3. Schematic diagram of SOI-MOS transistor with and without body-ties (Adapted from K. Hirose *et. al.* [12] [13])

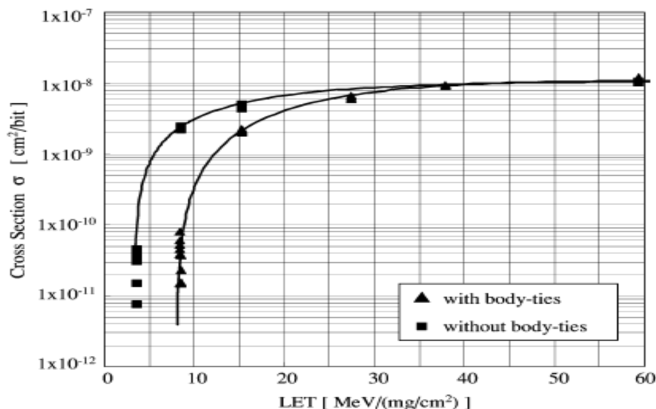

Fig. 4. Measurements of the SEU cross-section curves of a 128kb SRAM with and without body-ties (Adapted from Kerry Bernstein *et. al.*[12] [13])

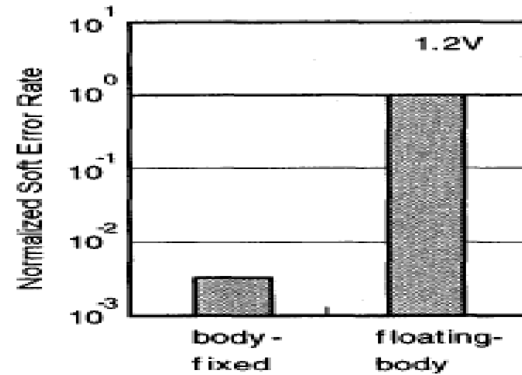

Fig. 5. Soft error rate of the body-fixed and the floating-body SRAMs (Adapted from Kerry Bernstein *et. al.* [7])

B. Introducing Dead Layer

Several techniques ranging from alternate process techniques to circuit design have been proposed [14] to improve SEU reliability. Significant reliability improvement was shown by introducing a dead layer of large p+ concentration underneath the transistor active region. This layer reduces the charge collection efficiency of radiation generated carriers on the sensitive junctions (drain of off NMOS of a SRAM cell) which in turn increases SEU reliability. The penalty is a marginal increase in circuit delay which can be tolerated due to simplicity of the proposed technique. This can be adopted easily in the prevalent VLSI process sequence.

C. Thin Layer between Isolation and Buried Oxide

In high density PD-SOI SRAM's, the body contact will be essential to reduce soft error rates. SOI SRAM with faster speed and higher soft error immunity than the bulk CMOS at low voltage can be realized by the well layer body contact structure [15]. As shown in Fig. 6 a thin well layer left between the isolation and the buried oxide can provide a convenient body contact layer that has no area penalty and is compatible with the bulk CMOS. T. Ikeda *et. al.* [15] estimated the body contact resistance required for soft error improvement through a device simulation. The error rate of the SOI SRAM was improved by about 2 orders of magnitude superior to the bulk device. Lower well resistance samples showed a little better soft error rate.

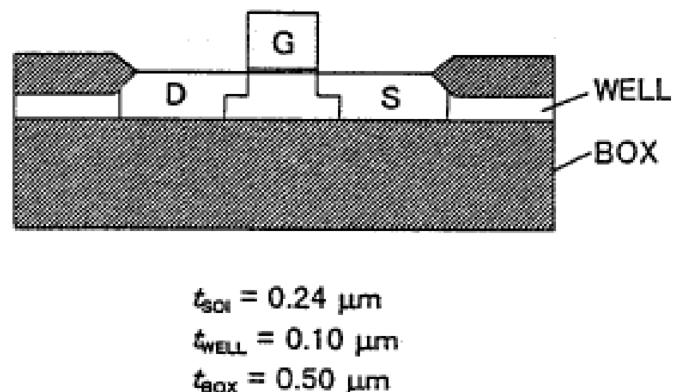

Fig. 6. SOI Device structure (Adapted from T. Ikeda *et. al.* [15])

D. Introducing Life Time Killers

It has long been recognized that the SEU sensitivity of SRAM cells fabricated on PD SOI technology will increasingly worsen for shorter channel lengths, due to the increasing significance of floating body effects [4] [16] and the parasitic bipolar transistor. Ioannou *et. al.* [16] [17] in 2003 reported a work to weaken the FBE and BJT roles through the incorporation of appropriate lifetime "killers" in the cell fabrication process, i.e. by incorporating appropriate delay elements. These lifetime killers must be chosen very carefully so that the desirable level of recombination lifetime reduction is achieved, while maintaining long generation lifetime to avoid large leakage currents. Fig. 7 is the schematic of the SRAM cell, including the parasitic BJT and a current source connected between drain and body of the OFF nMOSFET. More than 50% reduction in the value of β was achieved [16].

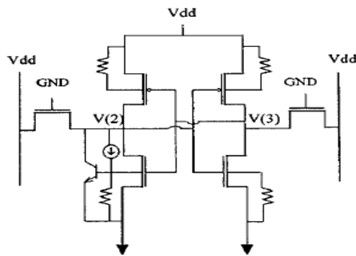

Fig. 7. 6T SRAM cells as used for SPICE simulations (Adapted from D.P.Ioannou *et. al.* [16])

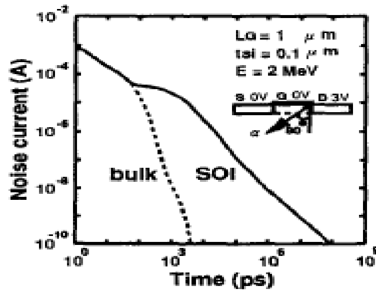

Fig. 8. α-particle induced noise currents for SOI and bulk nMOSFETs calculated using 3D device simulator. The difference corresponds to the bipolar currents. (Adapted from Yoshiharu Tosaka *et.al.* [8] [15])

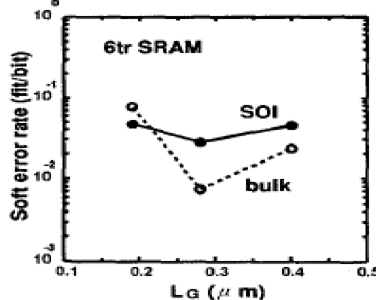

Fig. 9. soft error rates in SOI and bulk SRAMs as a function of effective gate length. (Adapted from Yoshiharu Tosaka *et.al.* [8])

E. Introducing Hardening Element

D. P. Ioannou *et. al.* [18] reported use of hardening element as shown in Fig. 10. All transistors in the cell are body-tied, and Rbsn, Rbsp account for the distributed body resistance of the nMOS and pMOS devices, respectively. Fig. 11 shows the critical charge dependency on the body resistance and it can be used as a guideline for designing for optimum SEU robustness. Further improvement on the cell immunity to SEU was obtained through the protection scheme of Fig. 10 where a transistor-resistors parallel combination was utilized as the hardening element (HE) [18].

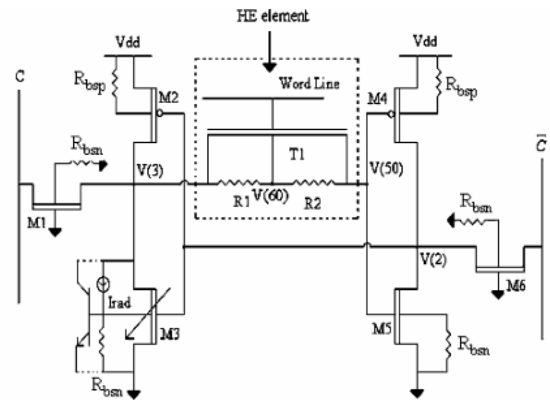

Fig. 10 Six-transistor SRAM cell with optional transistor T1 as a hardening element (HE). (Adapted from D. P. Ioannou *et. al.* [18])

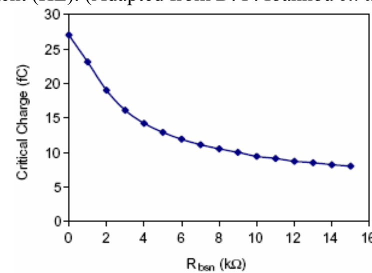

Fig. 11. Qcritical vs. body resistance. (Adapted from D.P.Ioannou *et. al.* [18])

F. Introducing Resistor Transistor Cross Coupling

SRAM cell that uses a gated resistor/transistor [19] in the cross coupling shown in Fig. 12 to obtain a high level of resistance to upset over temperature while maintaining a minimum worst-case write pulse of less than 20 ns when implemented in a 256K SRAM with 1.0μm SOI technology. The contribution of resistance and capacitance provides good SEU protection while not severely limiting the memory write time or cell area. Modeling does show that higher bipolar gain than that measured on a sample from the SRAM lot would produce a lower error rate. The worst-case supply voltage for SEU is primarily caused by the drain voltage dependence of the beta of the SOI parasitic bipolar transistor. SEU experiments with SOI devices should include measurements as a function of supply voltage to determine the worst case condition [19].

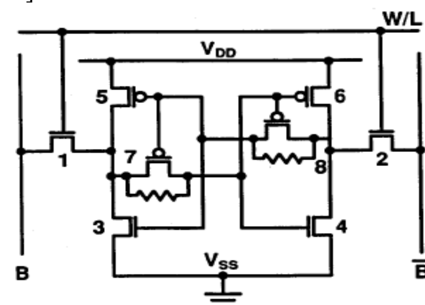

Fig. 12. Memory Cell Schematic. (Adapted from L. R. Hite *et. al.* [19])

G. Introducing Feedback Resistor and Capacitor

K. Hirose *et. al.* [13] used n and p type MOS transistors have body ties, as shown in Fig. 13, of the source-tie type, which are designed to reduce the leakage current in commercial products for low-power applications. The body ties can also reduce the parasitic bipolar effect, even in the present fully depleted SOI SRAM, by pulling the radiation-induced current out of the body silicon region, thus increasing the SEU resistance, although body ties are known to be much more effective for partially depleted SOI SRAMs with a relatively high bipolar gain. Feedback resistors R and capacitors C were placed as shown in Fig. 13 to improve the SEU resistance of the 128-Kbit SRAMs. The resistive and capacitive feedback hardening method [13] is more effective for SOI devices than for bulk devices since the time constant for time discrimination to preclude SEU is much shorter for the SOI device than for the bulk device. The time is shorter because of the lack of prompt funneling components and delayed diffusion components in the ion-induced current pulse.

The gate region of the access MOS became an SEU-sensitive area. Note that the access transistor suffers from upsets [13]. We tentatively assume that the upset in the access transistor is due to the ion-current-induced reduction of off-resistance in the access transistor compared with on-resistance in the nMOS [13].

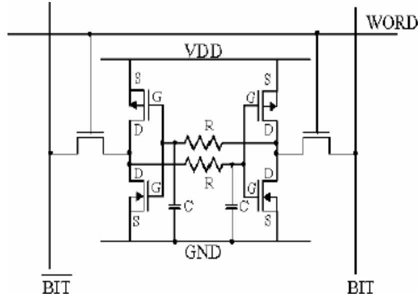

Fig. 13. Schematic layout of a 128-Kbit SRAM unit cell (Adapted from K. Hirose *et. al.* [13])

H. Using Active Delay Element (ADE) in Feedback Loop

It was reported [20] in 2003 that proton induced upsets in certain radiation hardened CMOS/SOI SRAMs can be attributed to a "double-hit" mechanism in which the upset is caused by a secondary heavy ion hitting a critical device as well as hitting the hardening element.

In a hardened SRAM cell where an active delay element [20] shown in Fig. 14 is often used in the feedback loop, single particle hits to a single critical node are not likely to cause an SEU upset. However, when the secondary heavy ions, created by the interactions between high-energy protons and Si nuclei, travel through a critical node as well as the pass gate inside the delay element, the delay element will be shunted out by charge deposited and as a result the stored state can easily be disturbed. Simple calculations based on this assumption yield good correlation to test results in .terms of upset cross-section. This upset mechanism will play a more important role as device geometries shrink.

However, H. Y. Liu *et. al.* [21] in 2006 have shown Si recoils are created by the primary beam, some of which travel as far as 4μm in the Si plane, with energy as high as 8Mev. It is shown that these Si recoils are the primary cause for the upsets observed in heavy ion testing of our CMOS/SOI SRAM test chip. During heavy ion bombardment such Si recoils traveling horizontally in the Si plane can hit both a critical node and the ADE (active delay element such as depicted in Fig. 14), and thus will disturb the state stored in the memory cell [21].

Saturated proton upset cross section for 6T SOI SRAM cells can be predicted [22] based on a simple

$$\sigma_{proton_upset} \approx \sigma_{heavy_ion_upset} N\sigma R = 1.38 \times 10^{-6} \sigma_{heavy_ion_upset}$$

This $\sigma_{heavy_ion_upset}$ can be estimated from layout and technology parameters. This approach provides a reasonable means to estimate the saturated proton upset cross section from layout and technology parameters. S.T.Liu *et. al.* [23] reported introduction of extra sensitivity at the low LETs due to the presence of the shunting transistor used in the delay element and is still under investigation.

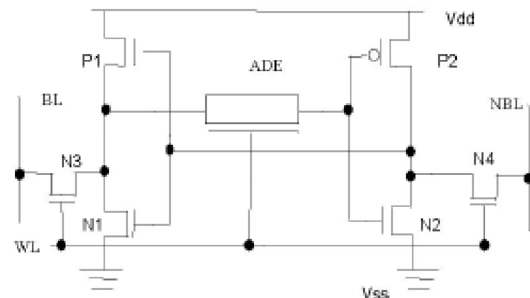

Fig. 14. SRAM cell with ADE (Adapted from S.T.Liu *et. al.* [20])

IV. DISCUSSION

A. Critical Parameters

Soft error upsets become more likely at lower voltages, both in SOI and in bulk. SOI just doesn't get as bad as quickly. At nominal voltages, SOI SER of an SRAM cell may have a 2X advantage over the SER of a bulk cell with identical dimensions. At reduced voltages for a given partially-depleted technology, that advantage may increase to 20X. Although at lower voltages SER in general increases, the SOI SER advantage over bulk becomes substantial, depending on device design point [7].

The mechanism for single-event upset of SOI pMOS, which can be more significant in SRAM when gate length is scaling down, can be associated with displacement current [24]. Displacement currents across the box layer can be induced as charge is generated in the SOI substrate by an ion strike. It perturbs the electric fields in the substrate near the oxide/substrate interface, thus an abnormal current is observed in drain. The displacement current is related to the box layer thickness, the substrate doping species and concentration, also the drain area. Therefore all this parameter is critical in the design of SOI SRAM ICs. The collect current is more significant when drain area is large. Therefore in SOI SRAM

ICs design, certain type of substrate must be considered first to avoid the depletion. Then the thickness of box layer, the substrate doping concentration, the active drain area should also be considered carefully [24].

B. Front vs. Back Exposure

To examine SEU asymmetry 0.15µm 64-Kb PD SOI SRAM with conventional 6T-cells were exposed to heavy ions, 14 MeV neutrons, and protons [25]. Upsets were measured, the LET threshold established and the upset cross sections determined for neutrons and protons. The SRAM's were rotated 180 and further exposed to neutrons. As shown in Fig. 15 there was a significant difference in the number of upsets from front versus back (or substrate silicon) exposure. The number of upsets from front exposure was more than double the number from back exposure. Following neutron exposure, proton upset measurements were performed [25]. For a given fluence, the number of proton induced upsets was essentially identical to the number of neutron induced upsets.

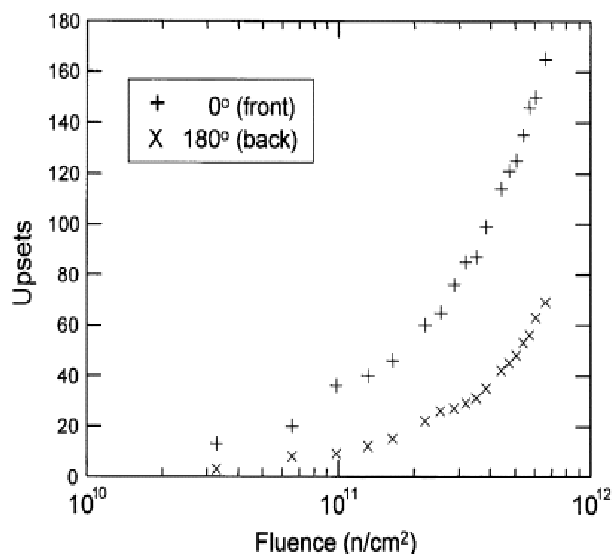

Fig. 15. Upsets from front and back 14 MeV neutron exposures of a SOI SRAM. (Adapted from P. J. McMarr *et. al.* [25])

C. Effect on SER Due to Process Variations

Tino Herjmen and Bram Kruseman [2] investigated the alpha-particle-induced soft-error rate (SER) of embedded SRAM's with a focus on the spread in SER owing to variations in the process parameters. The SER in both 0.18 and 0.13µm processes show design-to-design and batch-to-batch variations. In addition, the 0.13 µm SRAM's show a variation in SER between individual samples from the same batch. The use of the high-VT process option can reduce SER, because of a decrease in the collection of induced charges. These results illustrate the importance of accurate simulation methods and stress the need to test several samples, batches, and designs in order to characterize the SER of a specific type of SRAM.

This result [2] [26] shows that the impact of process variations on the spread in SER of embedded SRAM is growing. As a consequence, several designs, multiple batches per design, and multiple samples per batch have to be tested in order to obtain an accurate prediction of the nominal and worst-case SER for an SRAM compiler. An alternative would be to calculate SER data by simulation [2]. However, current state-of-the art simulation approaches are not (yet) capable of providing highly accurate SER data. The application of the high-V_T process option results in a lower SER compared to standard V_T SRAM, due to a change in the charge collection efficiency. The detailed explanation of this effect is a subject of further research. This result stresses the need for more advanced simulation techniques than currently available [2]. This is becoming increasingly important as the SRAM SER per mm^2 of memory is approximately doubling with every new technology generation.

D. Multiple Bit Upsets

Multiple Bit Upsets (MBU) must also be considered [3] in nanoscale technologies where a single alpha strike may intersect the SV of multiple cells. Theoretically, MBU should increase from the 90-nm node where the gate length and the radius of alpha-induced charge column become comparable. MBU calculated for SOI technologies is low, although it increases with technology downscaling. The authors would conclude that the SEU rate for the 65-nm SOI node would not significantly increase with the MBU contribution. Additional 3-D device simulations will be required to provide accurate quantitative MBU characterization. Devices manufactured with SOI processes have an advantage of lower charge sharing and lower rates of MBU.

E. Simulation and Modeling of SER

The SER measured with older technologies show that additional key parameters are needed to model the SER susceptibility of ultra deep submicron technologies. P. Roche *et. al.* [3] modeled key parameters controlling SER using Monte Carlo simulations to predict SER. Once calibrated, this model can quantify the relative influence of key parameters, such as the critical charge, the sensitive volume, and the charge sharing effect. For this later parameter, several memory cells are modeled in contiguous 3-D geometric and device domains, to explore the impact of multiple bit upsets. P. Roche *et. al.* [3] also shown how alpha-induced carriers spread between four contiguous SRAM devices.

The SER of a device in operation must consider contributions from both neutrons and alpha particles. P. Roche *et. al* [3] used SER alpha simulator, well-known rectangular parallelepiped parallelogram (RPP) model, since it can accurately represent the specific topology of the SOI process. A strong exponential SER increase with the operating voltage reduction was reported, with a slope equal to 2.1–2.2 FIT decades/V. The critical charge is definitively a necessary, but not sufficient, parameter to predict SER trends with technology. SOI SRAM's are less sensitive to power supply variations, with a slope of 0.5 decades/V at the 130-nm node, two to three times lower than Bulk for the same generation [3].

An additional key parameter is needed to describe SER trends with technology. The authors in [3] identify this parameter as the sensitive volume. The SV can be imagined beneath the most sensitive regions of each memory cell: the reverse biased drain of the drive N transistor. The sensitive volume determines the level of the SER susceptibility at saturation. The highest SER saturation level is observed for Bulk 250nm and the lowest for SOI 130nm. If future technologies reach the saturation region, the critical charge (and applied voltage) effect will become negligible and the SER will then only be driven by the SV dimensions. Simulations that included SV effects explain the observed trend that smaller technologies are less sensitive to voltage variations (have lower SER [voltage] slopes).

Simulations also demonstrate that SV effects can describe why SOI is less sensitive to power supply variations than Bulk, because the critical charge for SOI is reduced (compared with the same Bulk technology generation) by both bipolar amplification and lower capacitances. Upset efficiency of alpha strikes. This indirect parameter is defined [3] as the ratio of alpha particles that induce errors compared with the total number that cross the SV. This upset efficiency is determined by the critical charge and the bipolar amplification for SOI. Upset efficiency of both SOI and Bulk begins to saturate below the 130-nm node. When the upset efficiency becomes constant, the SER should therefore decrease for smaller technologies.

Alpha particles (which are directly ionizing) and neutrons (where only the collision products with the lattice nuclei are ionizing) are two distinct mechanisms for the charge collection that results in a soft error [3]. Neutron SER contribution is higher than that from alpha particles between 0.8 V and 1.8 V applied, with increased neutron SER contribution at higher voltage to the ratio of SER from neutrons to those from alpha particles is nine times at 1.8 V for both Bulk and SOI, and reduces to 1.5 times (Bulk) or three times (SOI) at 0.8 V. SER must include charge sharing effects that also depend on the sensitive volume. Additional modeling is required to extend these results to SER from neutrons [3].

Craig Lage *et. al.* [27] presented a quantitative model which attributes most soft errors in dense SRAM’s not to alpha particles as is commonly accepted, but to cosmic ray events. Cosmic ray events have become the dominant type of soft error in advanced SRAM’s, for two reasons. First, as device geometries have scaled down, doping concentrations have increased, reducing the funneling length of incident alpha particles, thereby reducing the charge collected from an incident alpha particle. Second, improvements in purity of semiconductor materials have reduced the flux of alpha particles in a typical circuit. The only practical protection against these cosmic ray point charge bursts is to have sufficient stored charge to keep the rate of such events at an acceptable level. A simple method of increasing the stored charge is to add capacitance i.e. adding a poly capacitor plate. Craig Lage *et. al*. [27] also elucidated the stored charge required in SRAM cells to achieve acceptable soft error rates. Enhancements to add capacitance are necessary at the 4 Megabit level and beyond.

Charge-collection and SEU experiments by P. E. Dodd *et. al.* [28] on 64 K and 1 M SOI SRAM’s indicate that drain strikes can cause single-event upsets in SOI ICs. 3-D simulations do not predict this result, which appears to be due to anomalous charge collection from the substrate through the buried oxide. This substrate charge-collection mechanism can considerably increase the SEU-sensitive volume of SOI SRAM’s, and must be included in single-event models if they are to provide accurate predictions of SOI device response in radiation environments.

F. Other Issues

The soft and hard errors in bulk and SOI SRAMs were investigated by proton probe irradiation with energies between 300 and 800 keV by Satoshi Abo *et. al.* [29]. In bulk SRAM, the hard errors occurred in the control circuits by latch up and less soft errors occurred in the SRAM cells. In SOI SRAM, the soft errors occurred in the SRAM cell by the floating body effect. The SER in SOI SRAM depends on the generated charge in the SOI body by proton probe irradiation. The soft errors in SOI SRAM’s are suppressed by a higher operating voltage at and near the normal operating voltage [29].

The performance and radiation data by Brady *et. al.* [9] for 256K SOI SRAM, Loral SOI technology, based on 0.5µm accumulation mode devices shows 30% decrease in the critical charge to upset relative to bulk CMOS. However further work is needed to clarify and understand the interaction of high energy ionizing particles with fully depleted accumulation mode devices [9].

In SOI static SRAM only ion-induced charge deposited under the gate that means in the body is supposed to contribute to SEU. However, recent works have shown that charge collection and then SEU could come from area other than the body [30]. Then SOI advantages against SEU in comparison to bulk technologies might not be as significant as it was claimed up to now. Thus it is important to study and understand SEU sensitivities in SOI technology in submicron region. For SOI cell, the most sensitive zone appears to be the body. Moreover, the threshold LET’s of tracks generated in the perpendicular to drain source direction are lower than the ones obtained in the drain source direction (the behavior is opposite for bulk technology). The sensitivity for tracks passing under the both off-transistors is higher than the one of each off-transistor considered separately. Here again, behavior is opposite of the bulk technology. Therefore, the case of SOI technologies has to be considered in a different way than the one of bulk technology. In other respects, future studies of SOI technologies will certainly require the improvement of the oxide modeling in device simulators [30].

V. CONCLUSIONS

The development of advanced methodologies to characterize and improve the SER of deep-submicron ICs is essential to assure product reliability. Further investigations are obviously required to better understand the mechanisms of the neutron-induced soft errors.

Using a radiation hard circuit design together with commercial SOI foundry processes is a promising approach for developing radiation hard application specific integrated circuit for future high-performance space systems. A radiation hard standard cell library for the present SOI technology should be developed for fabricating radiation hard ASICs, such as microprocessors. The promising technique for meeting the ASIC requirements of advanced space systems at low cost should be developed.

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VII. REFERENCES

[1] James B. Kuo and Shih-Chia Lin, "Low Voltage SOI CMOS VLSI Devices and Circuits," 1st ed., New York: John Wiley & Sons, 2001, pp. 299-200.

[2] Tino Heijmen and Bram Kruseman, "Alpha-particle-induced SER of embedded SRAMs affected by variations in process parameters and by the use of process options", Science Direct, Solid State Electronics, No. 49, pp. 1783-1790, 2005.

[3] P. Roche, G. Gasiot, K. Forbes, V. O'Sullivan, and V. Ferlet, "Comparisons of Soft Error Rate for SRAMs in Commercial SOI and Bulk Below the 130-nm Technology Node", IEEE Trans. On Nuclear Science, Vol. 50, No. 6, pp. 2046-2054, Dec. 2003.

[4] D.J. Schepis, F. Assaderaghi, D.S. Yee, W. Rausch, R.J. Bolam, A.C. Ajmera, E. Leobandung, S.B. Kulkami, R. Flakd, D. Sadana, H.J. Hovel, T. Kebede, C. Schiller, S. Wu, L.F. Wagner, M.J. Saccamango, **S.** Ratanaphanyarat, J.B. Kwlg, M.C. Hsieh, K.A. Tallman, R.M. Martino, D. Fitzpatrick, D.A. Badamit, M. Hakey, S.F. Chu, B. Davari, and *G.G.* Shahidi, "A 0.25µm CMOS SOI Technology and its application to 4 Mb SRAM", IEEE IEDM Technical Digest, Vol., pp. 587-590, 1997.

[5] Ching-Te Chuang, Pong-Fei Lu and Carl J. Anderson, "SOI for Digital CMOS VLSI: Design Considerations and Advances", IEEE Trans., Vol. 86, No. 4, pp. 689-720, April 1998.

[6] Masanao Yamaoka, Kenichi Osada, Kiyoo Itoh, Ryuta Tsuchiya, and Takayuki Kawahara, "Dynamic-Vt, Dual-Power-Supply SRAM Cell using D2G-SOI for Low-Power SoC Application", in *Proc.* Dec. 2004 IEEE International SOI Conference, pp. 109-111.

[7] Kerry Bernstein and Norman J. Rohrer, "SOI Circuit Design Concepts," 1st ed., New York: Kluwer Academic, 2002, pp. 141-144.

[8] Yoshiharu Tosaka, Kunihiro Suzuki, and Toshihiro Sugii, "α-Particle-Induced Soft Errors in Submicron SOI SRAM", Symposium on VLSl Technology Digest of Technical Papers, p.p. 39-40, 1995.

[9] F. T. Brady, T. Scott, R. Brown, J. Damato, and N.F. Haddad, "Fully-Depleted Submicron SOI For Radiation Hardened Applications", IEEE Trans. On Nuclear Science, Vol. 41, No. 6, pp. 2304-2309, Dec. 1994.

[10] F. Brady, B. Keshavan, and L. Rockett, "Evaluation Of The Performance And Reliability A 1m Sram On Fully-Depleted SOI", n *Proc.* Oct. 1998 IEEE International SOI conference, pp. 129-130.

[11] Yoshiki Wada,Koji Nii, Hirotada Kuriyama, Shigenobu Maeda, Kimio Ueda and Yoshio Matsuda, "A 128Kb SRAM with Soft Error Immunity for 0.35µm SOI-CMOS Embedded Cell arrays", in *Proc.* Oct. 1998 IEEE International SOI Conference, pp. 127-128.

[12] K. Hirose, H. Saito, S. Fukuda, Y. Kuroda, S. Ishii, D. Takahashi, and K. Yamamoto, "Analysis of Body-Tie Effects on SEU Resistance of Advanced FD-SOI SRAMs Through Mixed-Mode 3-D Simulations", IEEE Trans. On Nuclear Science, Vol. 51, No. 6, pp. 3349-3353, Dec. 2004.

[13] K. Hirose, H. Saito, Y. Kuroda, S. Ishii, Y. Fukuoka, and D. Takahashi, "SEU Resistance in Advanced SOI-SRAMs Fabricated by Commercial Technology Using a Rad-Hard Circuit Design", IEEE Trans. On Nuclear Science, Vol. 49, No. 6, pp. 2965-2968, Dec. 2002.

[14] P. K. Saxena and N. Bhat, "Process technique for SEU reliability improvement of deep sub-micron SRAM cell", Science Direct, Solid State Electronics, No. 47, pp. 661-664, 2003.

[15] T. Ikeda, S. Wakahara, Y. Tamaki, and H.Higuchi, "A Soft Error Immune 0.35µm PD-SOI SRAM Technology compatible with bulk cmos", in *Proc.* Oct. 1998 IEEE International SOI conference, pp. 159-160.

[16] D. P. Ioannou, S. Mitra, D. E. Ioannou, S.T. Liu and W.C. Jenkins, "Minimizing the Floating Body induced SEU sensitivity in a 0.35µ SOI SRAM cell through recombination lifetime control", IEEE Trans., pp. 83-84, 2003.

[17] Dimitris P. Ioannou and Dimitris E. Ioannou, "Beta engineering and circuit styles for SEU hardening PD-SOI SRAM cells", Science Direct, Solid State Electronics, No. 48, pp. 1947-1951, 2004.

[18] Dimitris P. Ioannou and Dimitris E. Ioannou, "Beta Engineering and Circuit Styles for SEU Hardening SO1 SRAM Cells", in *Proc* Dec. 2003 International Semiconductor Device Research Symposium, pp. 262-263.

[19] L.R. Hite, H. Lu, T.W. Houston, D.S. Hurta, and W.E. Bailey, "An SEU Resistant 256K SOI SRAM", IEEE Trans. On Nuclear Science, Vol. 39, No. 6, pp. 2121-2125, Dec. 1992.

[20] H. Y**.** Liu, S.T. Liu, K.W. Golke, D.K. Nelson, W. W. Heikkila, and W.C. Jenkins, "Proton Induced Single Event Upset In A 4M SO1 SRAM", IEEE Trans., pp. 26-7, 2003.

[21] H. Y. Liu, S. T. Liu and H. L. Hughes, "A new mechanism of heavy ion induced upset in SOI SRAMs", in *Proc.* 2006 IEEE International SOI Conference, pp. 123-124.

[22] Harry Y. Liu, Michael S. Liu, and Harold L. Hughes, "Proton Induced Single Event Upset in 6 T SOI SRAMs", IEEE Trans. On Nuclear Science, Vol. 53, No. 6, pp. 3502-3505, Dec. 2006.

[23] S. T. Liu, W. W. Heikkila, K. W. Golke, D. Anthony, A. Hurst, G. Kirchner, H. L. Hughes, S. Mitra and D. E. Ioannou, "Single Event Effects in PDSOI 4M SRAM Fabricated in UNIBOND", IEEE Trans. On Nuclear Science, Vol. 50, No. 6, pp. 2095-2100, Dec. 2003.

[24] Fa-Zhan Zhao, Tian-Lei Guo, Chao-He Hai and Meng-xin Liu, "Study of the SEU Effect Mechanism on SOI PMOS by 2-D Simulation", in *Proc.* Oct. 2006 8th International Conference on Solid –State and Integrated Circuit Technology ICSICT06, pp. 1346-1348.

[25] P. J. McMarr, M. E. Nelson, S. T. Liu, D. Nelson, K. J. Delikat, P. Gouker, B. Tyrrell and H. Hughes, "Asymmetric SEU in SOI SRAMs", IEEE Trans. On Nuclear Science, Vol. 52, No. 6, pp. 2481-2486, Dec. 2005.

[26] P. E. Dodd, F. W. Sexton, G. L. Hash, M. R. Shaneyfelt, B. L. Draper, A. J. Farino, and R. **S.** Flores, "Impact of Technology Trends on SEUI in CMOS SRAMs", IEEE Trans. On Nuclear Science, Vol. 43, No. 6, pp. 2797-2804, Dec. 1996.

[27] Craig Lage, David Burnett, Thomas McNelly, Kelly Baker, Al Bormann, Dean Dreier, Vince Soorholtz, "Soft Error Rate and Stored Charge Requirements in Advanced High-Density SRAMs", IEEE IEDM Technical Digest, p.p. 821-824, 1993.

[28] P. E. Dodd, M. R. Shaneyfelt, K. M. Horn, D. S. Walsh, G. L. Hash, T. A. Hill, B. L. Draper, J. R. Schwank, F. W. Sexton, and P. S. Winokur, "SEU-Sensitive Volumes in Bulk and SOI SRAMs From First-Principles Calculations and Experiments", IEEE Trans. On Nuclear Science, Vol. 48, No. 6, pp. 1893-1903, Dec. 2001.

[29] Satoshi Abo, Hiroto Yamagiwa, Toshiaki Iwamatsu, Shigeto Maegawa, Yutaka Arita, Takashi Ipposhi, Atsushi Kinomura, Fujio Wakaya and Mikio Takai, "Reliability study of bulk and SOI SRAMs using high energy nuclear probes", Science Direct, Nucl. Instr. and Meth. in Phys Res. B 231, pp. 482-485, 2005.

[30] K. Castellani-Coulié, B. Sagnes, F. Saigné, J.-M. Palau, M.-C. Calvet, P. E. Dodd and F. W. Sexton, "Study of an SOI SRAM Sensitivity to SEU by 3-D Device Simulation", IEEE Trans. On Nuclear Science, Vol. 51, No. 5, pp. 2799-2804, Oct. 2004.

VIII. Biographies

S. S. Rathod (M'2007) was born in Amravati in India on Feb 28, 1975. He graduated from Amravati University, and completed his post graduation in the field of Electronics Engineering from V.J.T.I., Mumbai-India. Currently he is pursuing his doctoral research at Indian Institute of Technology, Roorkee-India.

His employment experience includes eight years as an educationalist. He has published more that 20 papers in various national and international conferences. His special fields of interest include VLSI Design, process and device modeling. His name is listed in the science category of Marques Who's Who USA. He received several best paper awards and outstanding achievement ward (2007) by the Energy Society, India. He is member of IEEE, ISTE and ISNT.

S. Dasgupta (M'2007) was born in Varanasi in India on 1973. He has obtained Ph.d. in electronics from Banaras Hindu University in 2000. He has served at Indian School of Mines, Dhanbad, from 2000 to 2006. From 2006 Dr. Dasgupta is with Indian Institute of Technology Roorkee.

Dr. Dasgupta was reviewer of IEEE Transactions on Nanotechnology (2006), VLSI Design and Test Symposium (2003), International VLSI Design Conference (2004), VISION-2000. He is member of EDS, ISTE, IEEE and Institute of Nanotechnology. He received several honors that include Expert Committee Member to The Global Open University; The Netherlands, Senior Research Fellow (Department of Science and Technology, GOI), Marquis's Who's Who in Science in Engineering, USA.

Dr. Dasgupta has supervised Ph.D. thesis on Modelling and Simulation of Nanoscale Metal-Oxide-Semiconductor-Feild-Effect-Transistors, Modelling, Simulation and Design Issues of Nanoscale MOS Based Devices and Circuits and Nanoscale Memory Design. He has more than 30 papers in international conferences and 23 papers in international journals. He is handling sponsored project Special Manpower Development Project in VLSI from the Ministry of Human Resources and Development, GOI. His area of interest is Nanoelectronics, Nanoscale MOSFET modelling and simulation, Mesoscopic transport phenomenon, Design and development of low power novel architecture, Digital VLSI Design, Quantum Cellular Automata.

A. K. Saxena (M'2007) was born at Rampur (U.P.) in India on july 1st, 1950. Dr. Saxena obtained ***M.Sc.*** from ***Agra University*** in 1969 with third rank in undivided Agra University, ***M.Sc.(Tech.).*** from Department of Electronics and Electrical Engg.,***B.I.T.S.*** in 1971 with first rank, ***M.Engg.*** and ***Ph.D.*** from Department of Electronics and Electrical Engg.,***UMIST/Sheffield University*** (UK) in 1975 and 1978, respectively as one of the two ***Government of India National Scholars***. Served ***CEERI***, a sister laboratory of CSIR from 1972-74 working on semiconductor device technology and then served University of Roorkee (Now IIT-Roorkee) as Reader from 1978-88. Since 1988, he is a Professor in Solid State Electronics. He has also spent a year with Standard Telecommunication Laboratory (London) working on III-V compound characterization under pressure.

Dr. Saxena is a member of ***Overseas Advisory Board of IEICE Transactions of Electronics of Japan*** since 1992. He is also a Fellow, ***Honorary Editor and Member Editorial Board of IETE***, **one of the three Fellows** in semiconductors from India of ***Institute of Physics (London)*** and ***Chartered Physicist of Institute of Physics (London)***. The discovery of a level in ***GaAlAs*** is christened as ***'Saxena's Deep Donor'*** by ***Philips Research Laboratory***, Eindhoven (Netherlands)***.*** He is also a winner of ***INSA Young Scientist***, Roorkee University ***Khosla Award Gold Medal, Kothari Scientific Research Institute Award*** and ***S. K. Mitra Memorial Awards (twice) of IETE***. He is also a member of ***Research Board of Advisors of ABI (USA).***He has also been honored with the title of 'Man of the Year' by ABI (USA) and IBC (UK). He is also an ***expert member on many National Committees and referee for international journals/conferences.***

Dr. Saxena has been a Royal Society (London) - INSA visiting fellow and SERC (UK) senior visiting fellow at University of Surrey (UK).He was also awarded visiting fellowship by University of Michigan (USA). He has published about 150 research papers in international journals and conference proceedings with ***very high citation index***. He has also been Investigator-in-charge of several projects from DST, INSA, CSIR, UGC, etc. He also received financial assistance from NTT (Japan),IMT (Romania),DST, INSA, AICTE, DOE, UP Govt., Ministry of Education & Social Welfare and UOR/IIT for attending conferences abroad. Some of his research work has been included in books published from USA and Germany. His biography has been published in a large numbers of publications from U.K., U.S.A., Malaysia and India.

Dr. Saxena has supervised many Ph.D./M.E./M.Tech./M.Phil. theses in the area of metal-semiconductor ohmic and non-ohmic contacts, band structure and deep energy levels of GaAs, GaAlAs, GaP, InP, etc and quantum wells under pressure. He has also written ***AICTE sponsored nine volumes*** on the related subjects for working professionals.