

Studies on ASIC Design of High Frequency Low Power Photoreceiver using 0.15 μ m CMOS Technology

Shubhajit Roy Chowdhury and Mausumi Maitra

Abstract-- The recent convergence of fiber optic communication technology with VLSI circuit design methodologies has motivated the development of low power complementary metal oxide semiconductor (CMOS) photoreceiver capable of detecting optical pulses at 1Gbps. The current work focuses on the design of a fully integrated single beam photoreceiver that can accept optical pulses of 850nm wavelength at a bandwidth as high as 1Gbps suitable for implementation in fiber optic LANs and short haul optical interconnects. The receiver integrates a photo-detector and a preamplifier circuit. The idea of using the CMOS technology is to achieve a low power implementation of the system. The average power dissipation of the receiver has been found to be less than 0.105mW at a supply voltage of 1V. The current work has been done using the 0.15 μ m CMOS technology. Also, a comparative study of frequency response of the receiver circuit has been made for different values of junction resistance and capacitance of the p-i-n photodiode. The whole work has been done using TSPICE simulation tool.

Index Terms-- Photoreceiver, Preamplifier, Low power.

I. INTRODUCTION

FOR long distance optical communication, photoreceivers are implemented in III-V materials which exhibit a data rate of more than 20 Gb/s. The high cost of III-V photodetectors and optoelectronic integrated circuits (OEIC) exclude their use in short-distance applications like local-area-networks (LAN), optical interconnects etc. As the performance of complementary metal oxide silicon (CMOS) integrated circuits improves, the interest in using it in such cost-sensitive applications has risen. For these applications, operations at wavelengths near 850 nm is of interest because of the ready availability of the optical sources. As the high volume of low-cost OEICs will be needed in the coming years, research on photodetectors and OEICs is growing steadily. For instance, a hybrid OEIC with GaAs-Al-GaAs p-

i-n photodiode and 0.8 μ m CMOS amplifier was reported to operate at 625 Mb/s [1], whereas a GaAs photodiode and an amplifier in a 0.25 μ m CMOS technology showed a data rate of 1.25 Gb/s [2].

Several workers have identified the slow response times of integrated CMOS photodetectors as the major obstacle to high speed fully-integrated silicon-based receivers [3-6]. This is due to the long absorption length ($\sim 10 \mu$ m) for 850 nm light in Si coupled with shallow junction depths ($< 1 \mu$ m) of modern CMOS processes. Kuchta et al employed the buried collector of a BiCMOS process where the bulk generated carriers have been screened from the amplifier input and realized 622 Mbit/s operation [3]. Woodward et al used a similar concept based on the n-well of a standard CMOS process and obtained a receiver capable of 1 Gb/s operation [7]. Here we are presenting the TSPICE simulation of fully-integrated silicon-based receiver using 0.3 μ m CMOS technology which is capable to operate at 1 Gb/s with a power dissipation as low as 0.105 mW.

II. THEORY

A photodetector is an optoelectronic device that absorbs optical energy and converts it to electrical energy to photocurrent. At wavelength less than 1.0 μ m, the silicon with its highly developed technology is clearly the perfect choice. The absorption depth at 850 nm means that a depletion layer thickness of a few tens of microns is desirable. Silicon photodiodes are normally made with p-i-n structure, in which the epitaxial layer is so lightly doped that the depletion layer reaches through to the heavily doped substrate at the normal operating voltage. With the p-i-n structure the optimum wavelength, the operating voltage, the device capacitance and frequency response are determined during manufacturing. If the impurity concentration in the lightly doped I layer is sufficiently low, an almost uniform electric field extends across it. Quantum efficiencies of 0.8 or more can readily be obtained and can be optimized for a particular wavelength by varying the thickness of the epitaxial layer. Silicon photodiodes designed for the wavelength range 1.0-1.1 μ m where the absorption is weak (absorption co-efficient $< 10^4$) a very wide drift region is required and hence high bias voltage and very lightly doped materials have to be used.

In optical communication system at the receiver input the signal level is the weakest and the system S/N ratio sets a lower limit on the acceptable level of the received optical

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power. Therefore the design of the front-end amplifier is an important task because the sensitivity of the receiver very much depends on its performance. As the current is converted into voltage a transimpedance amplifier is used where the problem of limited dynamic range and the bandwidth are removed by employing a negative feedback. By increasing the feedback resistance the thermal noise can be reduced and hence the sensitivity can be improved. Again to extend the bandwidth the resistance has to be low. Therefore there should be a trade-off between this two.

III. SPICE MODELING OF THE PHOTO-RECEIVER

The SPICE model of the photoreceiver circuit has been shown in figure 1.

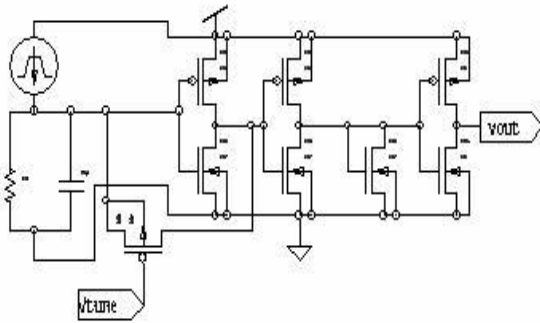


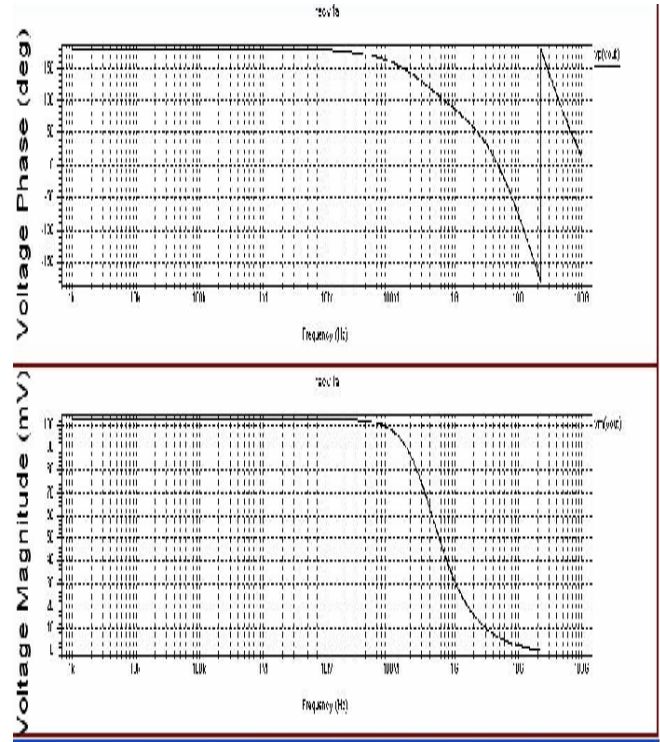
Fig. 1. Circuit diagram of the photo-receiver circuit using a SPICE model of the photodetector

The p-i-n photo-detector is modeled by its equivalent circuit consisting of a 5mA pulsed current source that is in series with a parallel combination of a resistance R and a capacitance C. The current source substitutes the photodiode which would detect input optical pulses arriving at a rate of 1Gbps and would generate current pulses to the input of the preamplifier section of the receiver circuit.

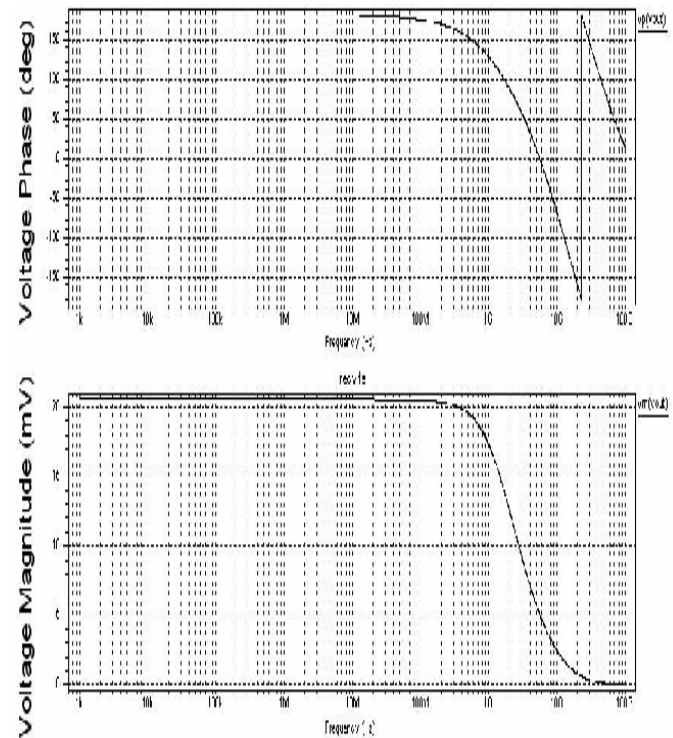
The photoreceiver consists of three distinct sections. The first stage is a push-pull inverter based transimpedance stage, using a PMOS transistor as the feedback element. The gate voltage of this FET can be adjusted for optimum performance at a given bit rate and optical power. The second stage is identical to the first with a diode connected NMOS load to reduce, broaden and stabilize the gain and switching threshold of this stage. The final stage is a high gain inverter acting as an asynchronous decision circuit which again is identical in geometry to the first two stages. The interaction between the feedback element of the transimpedance stage and the NMOS diode load of the second stage is key to the operation of the circuit defining the first stage transimpedance and the switching impedance and switching offset between the analog gain stages and the decision circuit necessary to permit single beam dc coupled operation. The W/L ratio of each transistor is kept at $0.9\mu\text{m}/0.3\mu\text{m}$. The supply voltage is set to 1V and the tuning voltage V_{tune} is set to 0.8V to maximize the gain around 1Gbps. CMOS push-pull inverter has been intentionally used at each stage to achieve a low power implementation of the system.

IV. SIMULATION AND RESULTS

Simulation has been done using the TSPICE simulation tool of the Tanner EDA tool suite. AC decade analysis of the receiver circuit has been performed for different values of the junction resistances and capacitances. The graphs for the AC analysis are shown in figure 2.



a. C=10pF, R=50 Ohms.

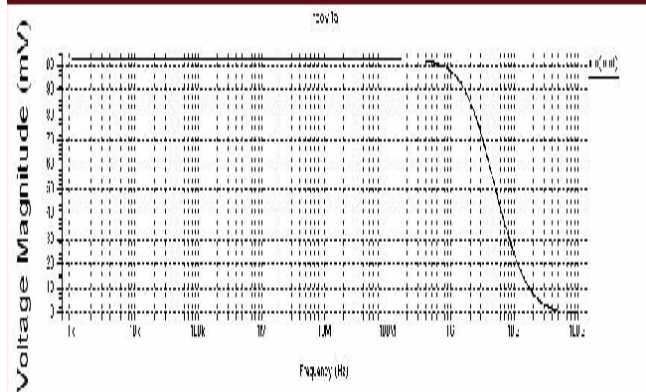
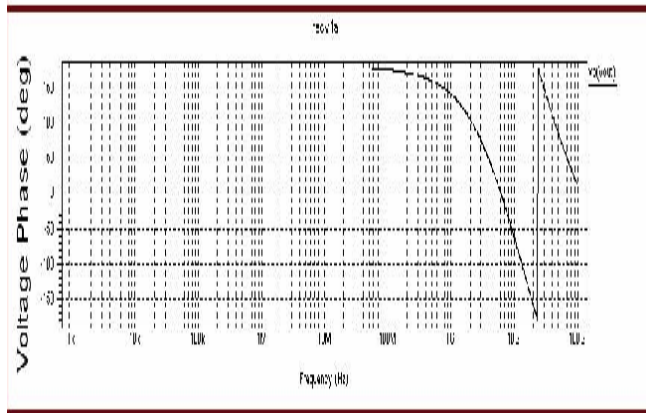


b. C=10pF R=10 Ohms.

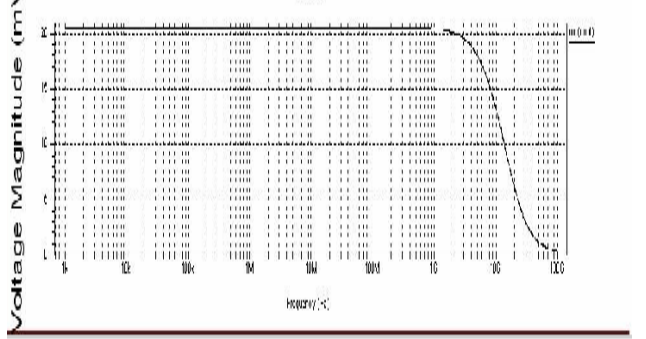
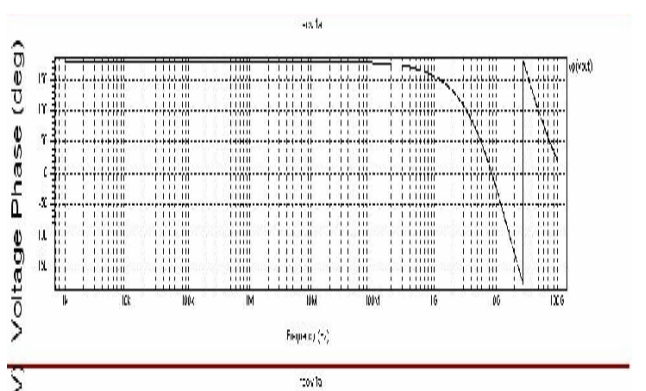
voltage which essentially proves that the output signal is not much distorted with respected with respect to the input signal. The power analysis of the circuit shows an average power dissipation of only 0.105mW.

TABLE I
COMPARATIVE STUDY OF THE BANDWIDTH OF THE RECEIVER

JUNCTION CAPACITANCE	JUNCTION RESISTANCE	BANDWIDTH OF THE RECEIVER
10pF	50ohms	600MHz
10pF	10ohms	2.5GHz
1pF	50ohms	5.0GHz
1pF	10ohms	13.0GHz



c. C= 1pF, R=50 Ohms



d. C=1pF, R=10 Ohms.

Figure 2. Results of ac analysis of the photoreceiver circuit showing the magnitude and phase response of the receiver for different values of C and R

Table-1 shows a comparative study 3-dB bandwidth of the receiver circuit. The phase response characteristic indicates an almost zero phase at the frequency of maximum output

V. CONCLUSION

In conclusion, we present the SPICE simulation of a fully-integrated optical receiver made entirely by 0.15 μm CMOS technology. Frequency and phase response show almost zero distortion at the 3-dB cut-off frequencies. Also, the low average power dissipation makes the design more attractive. Therefore, this ASIC design of CMOS optical receiver seems very promising for many low-cost short-range optical data transmission applications.

VI. REFERENCES

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VII. BIOGRAPHIES



Shubhajit Roy Chowdhury was born on August 27, 1981 in India. He received his B.E. degree in 2004 and M.E. degree in 2006 being Gold Medalist in both the examinations. He is currently pursuing his Ph. D at the IC Design and Fabrication Centre, Department of Electronics and Telecommunication, Jadavpur University. He is a member of VLSI Society of India and a life member of the Indian Statistical Institute and Indian Microelectronics Society. His current research interests span around

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