FPGA and ASIC Based System Design For Digital Signal Processor

Prasad A. Kulkarni and D.R. Mehta

Abstract--**Programmable logic offers an alternative solution for the computationally intensive functions found in Digital Signal Processing (DSP).Programmable logic can provide increased DSP system performance at reduced system cost .Programmable logic combines the flexibility of a general purpose DSP plus the speed ,density and low cost of an ASIC implementation .In some applications, programmable logic replaces the DSP processor entirely. In others, programmable logic works in conjunction with the DSP processor, offloading the computationally intensive function and freeing the processor for other function. Digital signal processing is the application of mathematical operation in digitally represented signal. The operation of Digital signal processor on input samples could be linear or non-linear, depending on the application of interest. The samples of the Signal are quantized to a finite number of bits. Signal processor can be either programmable or of dedicated nature. Digital signal processors have traditionally been optimized to compute FFT. Since processor have special instruction set i.e. Special Instruction Set Single Chip (SISC) computers. The processor is specially designed to meet the needs of parallel processing.[1]**

I. Introduction

MANY Electronic system making use of digital signal processing. Digital signal processing is the application of mathematical operation to digitally represented signals. Signals are represented digitally as a sequence of samples. Often these samples are obtained from physical signal (e.g. audio) through the transducers, A/D converters. After mathematically processing digital signals may be back to physical signals via D/A converters. In some systems the use of DSP is central to the operation of the system. The operation of digital signal processor on input samples could be linear or non linear, depending on the application of interest.

II. What is a Digital Signal Processor?

A digital signal processor (DSP) accepts one or more discrete time inputs $x_i[n]$, and produces one or more outputs $y_i[n]$, for n = …,-1,0,1,2, 3,4, . . .and i= 1, . . . ,N. The inputs could represent appropriately sampled (analog to digital conversion) values of continuous time signals of interest, which are then processed in the discrete time domain, to produce outputs in discrete time that could then be converted to continuous time, if necessary. The operation of the digital signal processor on the input samples could be linear or non-linear, time-invariant or time varying, depending on the application of interest. The samples of the signal are quantized to a finite number of bits, and this word length can be either fixed or variable within the processor. Signal processors operate on millions of samples per second, require large memory bandwidth, often requiring as many as a few hundred operations on each sample processed. These real-time capabilities are beyond the capabilities of conventional microprocessors and mainframe computers. Digital signal processors have traditionally been optimized to compute FIR convolutions (sum of products), IIR recursive filtering, and Fast Fourier Transform type (butterfly) operations that typically characterize most signal-processing algorithm. They also include interface to external data ports for real-time operation. These processors having specialized instruction sets are called as Special-Instruction Set Single Chip (SISC) computers.

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III. Why VHDL?

1. Using the same language it is possible to simulate as well as design a complex logic.
2. Design reuse is possible
3. Design can be described at various levels of abstractions.
4. It provides for modular design and testing.
5. The use of VHDL has tremendously reduced the “Time to Market “for large and small design.
6. VHDL designs are portable across synthesis across synthesis and simulation tools, which adhere to the IEEE 1076 standard.
7. Using VHDL makes the design device independent.
8. The design description can be targeted to PLD, ASIC, FPGA very easily.
9. Designer has very little control at gate level.
10. The logic generated for the same description may vary from tool to tool. This may be due to algorithm used by the tools, which might be proprietary.

IV. Advantages

Digital signal processing enjoys several advantages over analog signal processing.

Insensitivity to environment: - Digital systems, by their very nature, are considerably less sensitive to environmental conditions than analog systems.

Insensitivity to component tolerances: - Analog components are manufactured to particular tolerances. The overall response of an analog system depends on the actual values of all the analog components used. In contrast

digital component always produce the same outputs given by input.

Predictable, repeatable behavior: - DSP system output doesn't vary with environmental factor or component variation, it is possible to design system having exact , known response that do not vary.

Reprogram ability: - If DSP system is based on programmable processors; it can be reprogrammed-even in the field to perform other tasks.

Size: - The size of analog component varies with their values. In contrast, digital systems remain unchanged.

V. FFT DSP PROCESSOR

Digital signal processing is the application of mathematical operation in digitally represented signal. The operation of Digital signal processor on input samples could be linear or non-linear, depending on the application of interest. The samples of the Signal are quantized to a finite number of bits. Signal processor can be either programmable or of dedicated nature. Digital signal processors have traditionally been optimized to compute FFT. Since processor have special instruction set i.e. Special Instruction Set Single Chip (SISC) computers. The processor is specially designed to meet the needs of parallel processing.

VI. FEATURES OF FFT DSP PROCESSOR

1. 32 bit processor
2. 4 KB on chip RAM, ROM
3. 32 bit 16 registers
4. 32 bit communication port
5. Harvard architecture
6. 32 bit Floating point adder and multiplier

VII. ARCHITECTURE

The major component of processor includes ROM, RAM, ALU, and register file and course of controller. The Harvard architecture comprised simultaneous access of data and coefficient leading to efficient implementation of DSP algorithms. The register file which is connected to the out put of ALU, the multiplier, RAM, buses are also capable of performing two read simultaneously

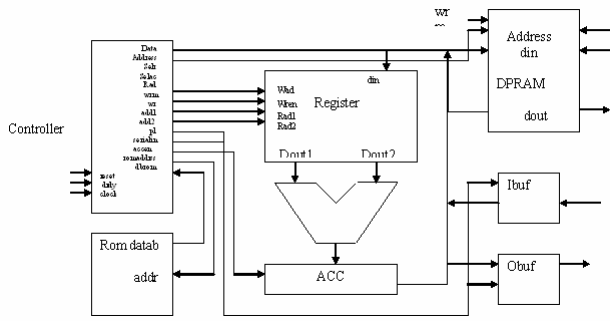

Figure 1.Architechure of FFT DSP Processor

VIII. RESULT AND SUMMARY

The users are given the flexibility to design and include their own custom hardware FPGA or ASIC based with their choice of processor whether it is on chip or off the chip. FPGA can provide superior performance to general purpose DSPs.

TABLE.1
FFT input in DPRAM

Sr.No.	Memory Address	Data	Remark
1	0000	00000000	Xe(0)=1
2	0001	02000000	Xe(2)=4
3	0010	01400000	Xe(1)=3
4	0011	01000000	Xe(3)=2
5	0100	01000000	Xo(0)=2
6	0101	01400000	Xo(2)=3
7	0110	02000000	Xo(1)=4
8	0111	00000000	Xo(3)=1

TABLE.2
OUTPUT IN DPRAM

Sr.No.	Memory Address	Data	Remark (Real)
1	0022	04200000	X(0)=20
2	0024	02C5A000	X(1)=-5.2
3	0026	80000000	X(2)=0
4	0028	FDCFFF0	X(3)=-0.172
5	002A	80000000	X(4)=0
6	002C	FDCBFF0	X(5)=-0.172
7	002E	80000000	X(6)=0
8	0030	02C58000	X(7)=-5.2
Sr.No.	**Memory Address**	**Data**	**Remark (Imaginary)**
1	0023	80000000	X(0)=0
2	0025	01E63FFF	X(1)=-2.4
3	0027	80000000	X(2)=0
4	0029	FEABFFF8	X(3)=-0.414
5	002B	80000000	X(4)=0
6	002D	FE4E008	X(5)=0.414
7	002F	80000000	X(6)=0
8	0031	011A8001	X(7)=2.414

IX. REFERENCES

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