A Novel Low Power High Speed Field Programmable Gate Array Routing Interconnects

Kureshi A. K, Naushad Alam and Mohd. Hasan

***Abstract*-- We propose a new energy efficient methods of designing switches and routing interconnects inside FPGA using novel variation of Dynamic Threshold MOS (DTMOS) instead of traditional NMOS pass transistor based switch and interconnects. The extra needed transistor can be easily shared in multiplexer based routing architecture of FPGA, which helps in keeping area overhead to be minimum. Extensive transistor level HSPICE simulation based on BPTM (Berkeley predictive technology model) for 65nm channel length device at operating frequency of 300MHz shows that during active mode using our new novel design, we obtain an average 18% improvement in power delay product (PDP) of simple switches (pass and tri-state buffer switches) and an average 26.75% improvement in the PDP of Virtex-II FPGA routing interconnects over conventional approaches. Since FPGA consists of thousands of Multiplexer based routing interconnects, hence the overall improvement in the PDP is significant.**

***Index Terms*-- Low power, High speed, Dynamic threshold-CMOS, FPGA routing switches, Interconnects.**

I. INTRODUCTION

THE leakage problem is the major obstacle for FPGA application in both high performance and low power embedded designs. Shrinking transistor channel lengths, reducing oxide thickness and dropping threshold voltage are all contribute towards the rapid increase in leakage power [1]. As power is related quadratically on the supply voltage, reducing the voltage to ultra-low level results in a dramatic reduction in both power and energy consumption. A study done on a state of art 90nm Virtex-II FPGA family from Xilinx shows that the interconnect is the dominant energy consumer, with hex lines, double lines and long lines consuming most of power [2]. If the energy consumed by the interconnect is reduced, it would contribute greatly to a reduction in the overall energy consumed by the FPGAs. Power consumption of FPGA is a vital design objective for portable devices such as mobile communication and bio-medical application where the power lowering is as important as the performance [3]. The basic switching element in most of FPGAs is NMOS pass transistor but it suffers from the threshold voltage drop and causes high DC power dissipation in level restoring buffer. To eliminate the problem of static power dissipation recent architecture from Xilinx and Altera Stratix FPGAs make the use of buffers [4], [5].]. However this approach has some disadvantage, replacing all pass transistor switches with tri-state buffers yields a significant increase in area and power consumption [6]. We show through our work, that there are some methods other than replacing the pass transistor by buffers for reducing energy consumption. The propose method using novel configuration of Dynamic threshold MOS (DTMOS) based switches overcome above disadvantage at a minimal increase in area.

Also through our work, we illustrate the type of switch configuration that needs to be chosen for meeting different performance constraints. Such as we make the main transistor (MT) of DTMOS switch as high Vt transistor so during the active mode the high Vt is reduced due to the body-source forward bias and during standby when the body-source voltage is zero the high Vt reduces the subthreshold leakage while maintaining an acceptable active power delay product [7]-[10]. Using this variation we can trade-off standby leakage versus active power delay product. All simulations are executed at 65nm BPMT technology at 300MHz [11].

The rest of this paper is organized as follows. Section 2 describes different schemes of DTMOS. Section 3 describes the implementation of proposed switches in Island-style FPGA routing architecture. Section 4 describes the implementation of proposed routing in Virtex-II FPGA architecture and section 5 concludes this paper.

II. DIFFERENT SCHEMES OF DTMOS

Fig.1 shows different symbol of DTMOS that works as

A. K. Kureshi is pursuing Ph.D. in the Electronics Engineering Department, Aligarh Muslim University, Aligarh-202002 India (e-mail: akkureshi@rediffmail.com).

Naushad Alam is with the University Polytechnic, Aligarh Muslim University, Aligarh-202002, India. (phone: +919897165051; e-mail: itsnaushad@rediffmail.com).

Dr. Mohd. Hasan is with the Electronics Engineering Department, Aligarh Muslim University, Aligarh-202002 India (e-mail: m_hasan786@rediffmail.com).

follows:

(a) Basic DTMOS: - it consists of single NMOS transistor, in which the body is connected to the gate terminal. The gate voltage swing cannot exceed the cut-in voltage of the diode otherwise a large current would flow through the forward-biased body-source and body-drain junction diodes. To overcome above limitation of DTMOS some variations have been proposed in the basic circuit, which are as follows [8].

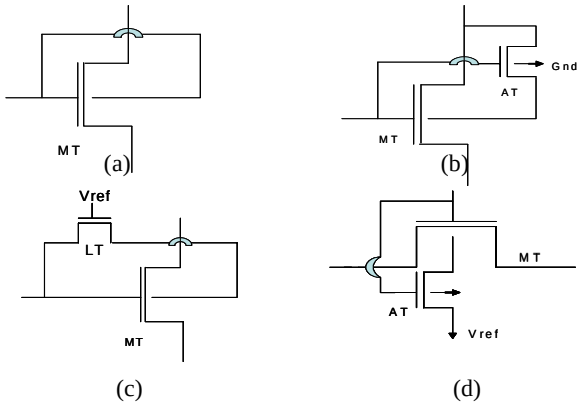

Fig.1 Symbol of different DTMOS

(b) DTMOS with Augmenting transistor: - it consists of main transistor (MT) and augmenting transistor (AT) the drain and gate terminal of both transistor are shorted to each other, hence it is not possible to share the augmented transistor between other main transistors.

(c) DTMOS with limiting transistor: - it consists of one main transistor (MT) and one limiting transistor (LT) the gate of LT is connected to the reference voltage (Vref). In the active mode the threshold voltage of MT is reduced by a magnitude of (Vref- Vt) only. The disadvantage of this scheme is that the limiting transistor is always on due to Vref at the gate terminal of LT, which increases the gate-oxide tunneling when the switch is inactive because of this reason the standby leakage of this scheme is highest among the all DTMOS schemes.

(d) DTMOS with Augmenting fixed reference voltage transistor: - it consists of main transistor (MT) and Augmented transistor (AT) a fixed reference voltage (Vref) is connected to the drain of AT. When MT is on a fixed body bias of (Vref- Vt) is applied to the MT as only the gate terminal of MT and AT are shorted hence it is possible to share a single AT between many MT transistor which is useful in multiplexer based routing switches. This scheme reduces the area penalty by a large margin. Through out this paper we have used the above scheme of DTMOS, which can be further configured as follows.

SS- this switch consume more energy the delay through this switch is less because both MT and AT are having nominal threshold voltage (Svt)

SH- the power consumption of this switch is lower than SS, due to high threshold voltage (Hvt) of AT there is certain delay in body biasing of MT therefore the propagation delay of SH is slightly higher than SS.

HS- due to Hvt of MT the propagation delay of this switch is higher than SH but the power delay product of this scheme is comparable to SH scheme.

HH- here both MT and AT are having high threshold voltage (Hvt) therefore the power consumption of this switch is lowest and delay is highest among all other DTMOS switch configuration. Between the trade-off of power and delay we have used the criteria of power delay product (PDP) to choose the best switch scheme among all proposed DTMOS switches.

III. ISLAND-STYLE FPGA ROUTING ARCHITECTURE

Fig. 2 shows an island-style FPGA routing architecture, Xilinx Spartan FPGA falls in this category. It consists of logic blocks and routing switches. The logic block has a basic logic element (BLE). The BLE consists of one K- input lookup table (K-LUT) and one flip-flop. A group of BLE forms a cluster, which is called configurable logic block (CLB). The connection between the logic blocks is made by using one wire or two wire programmable switches [12]. The routing switches are in the form of pass transistors (NMOS) and tri-state buffers [13]. This section implements the above two switches by using DTMOS technology and also compare there performance based on the lowest power delay product (PDP).

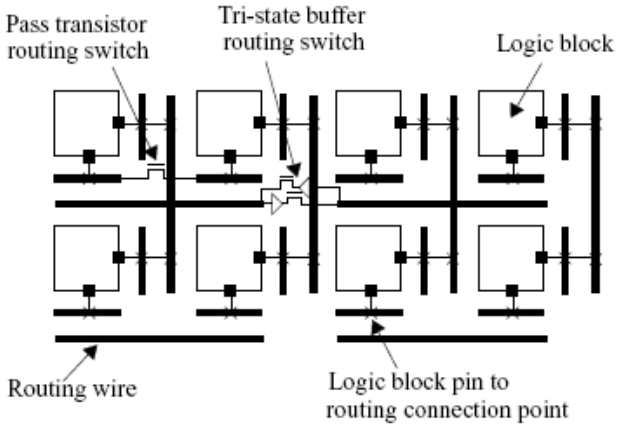

Fig. 2 Island-style FPGA routing architecture

A. PASS TRANSISTOR SWITCH

Fig 3 (a), (b) and (c) shows the power consumption, delay and power delay product of conventional and proposed DTMOS based pass switches respectively. Due to high threshold voltage (Hvt) of MT and AT transistor the power consumption of PHH pass switch scheme is least. The power delay product of this scheme at supply voltage (Vdd=0.7v) is marginally lowest among all other DTMOS configuration including the conventional pass transistor switch.

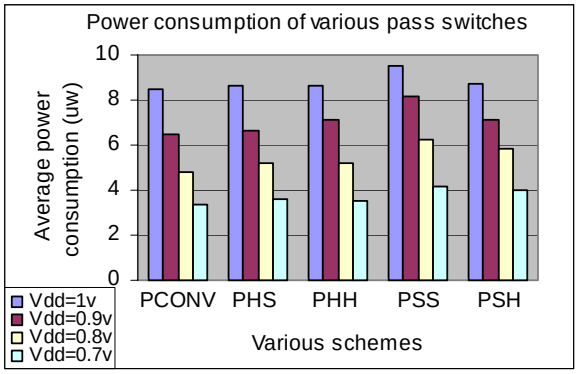

Fig.3 (a) Power consumption of various pass switches

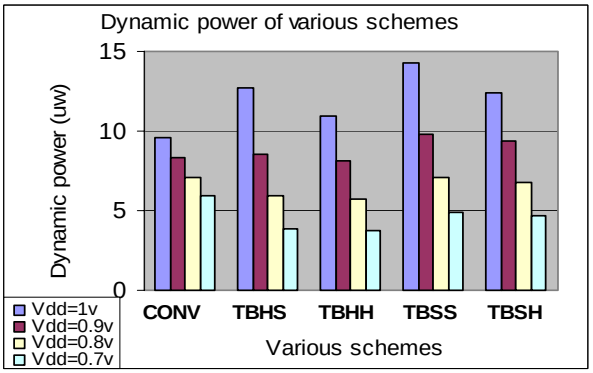

Fig.4 (a) Power consumption of various Tri-state buffer switches

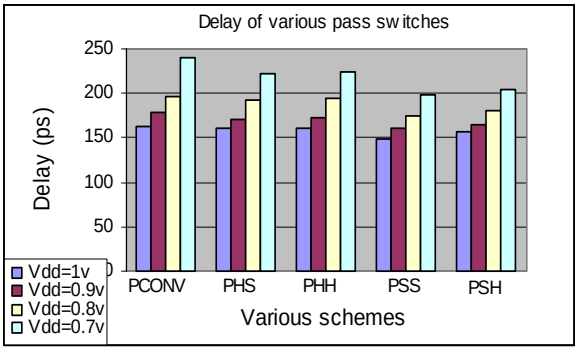

Fig.3 (b) Delay of various pass switches

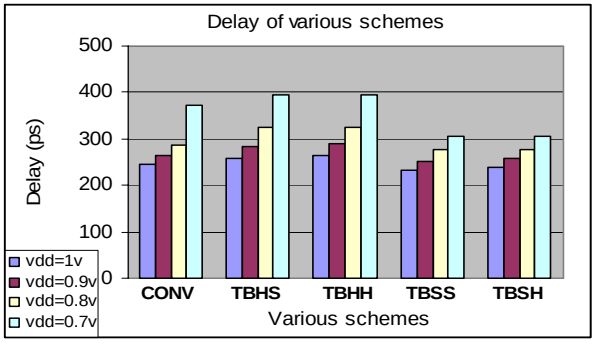

Fig.4 (b) Delay of various Tri-state buffer switches

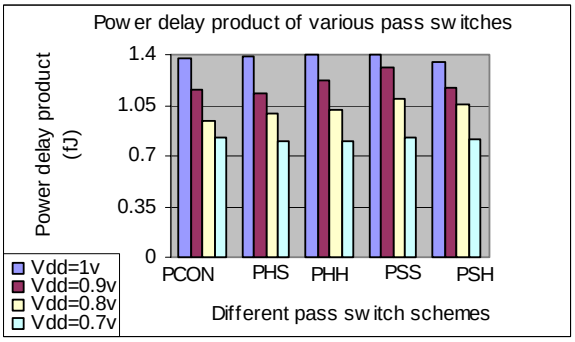

Fig.3 (c) Power delay product of various pass switches

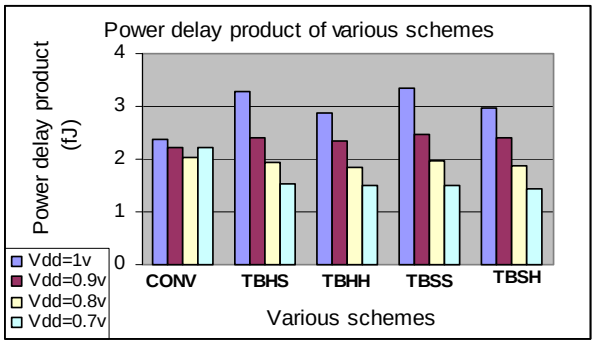

Fig.4 (c) Power delay product of various Tri-state buffer switches

B. TRI-STATE BUFFER SWITCH

When long connections are required pass transistors are unsuitable due to quadratic rise in delay, whereas buffers are slower for short connection and required more area. Fig 4(c) shows that our proposed DTMOS based tri-state buffers are more power efficient than the conventional buffers. At supply voltage (Vdd=0.7v) the power delay product (PDP) of proposed DTMOS based four tri-state buffers are approximately 32% less than the PDP of conventional tri-state buffers.

IV. VIRTEX-II FPGA ARCHITECTURE

We have chosen the island-style SRAM-based FPGA architecture for our study. Xilinx and Altera's FPGA fall into this category [14], [15], our experiments were performed on Xilinx Virtex-II FPGA as shown in Fig.5 The basic logic element in a Virtex-II is called a slice. A slice consists of 2 LUTs (Lookup-table), 2 flip-flops, fast carry logic and some wide multiplexers. A CLB in turn consists of 4 slices and an interconnect switch matrix.

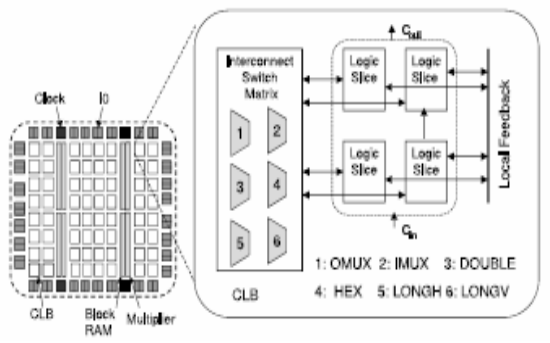

Fig.5 Virtex-II FPGA Architecture

The interconnect switch matrix consists of variable length wire segment that connect to one another through programmable buffered switches, such as IMUX (input multiplexer) selects and routes a signal to a slice input pin. The OMUX (output multiplexer) selects and routes a signal from a slice output pin to neighboring logic block. Double block drive wire segment that span 2 CLB tiles, HEX blocks drive wires that span 6 CLB tiles and long horizontal (LONGH) and vertical (LONGV) resources span the entire width or height of the FPGA. Table I lists the different interconnects in Virtex-II family FPGAs.

TABLE I
MAJOR INTERCONNECTS PRESENT IN THE SWITCH MATRIX

Circuit-Block	Details
IMUX	30-to-1 multiplexer and buffer
OMUX	24-to-1 multiplexer and buffer
DOUBLE	16-to-1 multiplexer and buffer
XEH	12-to-1 multiplexer and buffer
LONGH/LONGV	n-to-1 multiplexer and buffer

All interconnect consists of wide input NMOS transistor based multiplexers and a level restoring buffer. A threshold voltage (Vt) drop is lost across the device when it tries to pull the output high, this signal degradation subsequently slows the pull-down of the output buffer and causes a high leakage because the pull-up is not fully off. Since the DTMOS circuit potentially lower the on-state threshold voltage to zero or quite below Vt, therefore DTMOS based interconnects get benefited from such type of design. Fig 6 to 9 shows the power delay product (PDP) of HEX, DOUBLE, OMUX and IMUX interconnect respectively. At supply voltage (VDD=0.7v) the PDP of all DTMOS based interconnects are quite lower than the conventional interconnects this show that DTMOS based interconnects are more power efficient than the conventional interconnects. The proposed DTMOS based interconnects are slightly complex because the level restoring buffer requires positive as well as negative reference voltage (Vref) for the body-bias of NMOS and PMOS transistors.

V. CONCLUSION

In this paper, we demonstrate the various techniques of DTMOS that can be used for a broad range of supply voltages. DTMOS delay and efficiency become superior to the traditional design as the voltage is reduced and the loading is increased. Employing the proposed DTMOS based switches results in an energy-efficient FPGA architecture. Simulation results at supply voltage (Vdd=0.7v) and operating frequency (F = 300MHz) shows an average 18% improvement in the

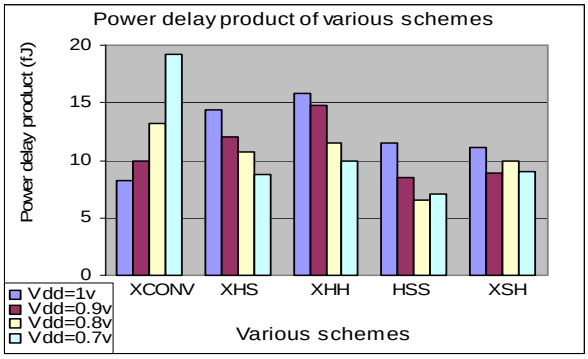

Fig.6 Power delay product of various HEX interconnect

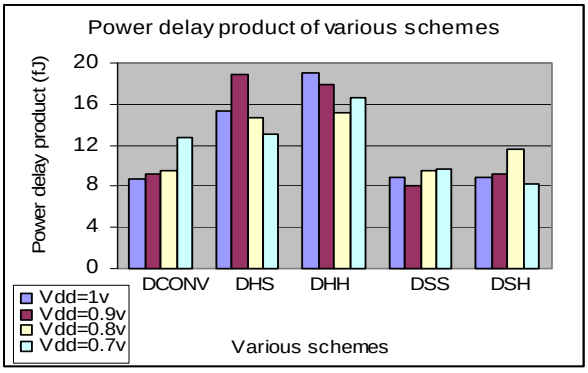

Fig.7 Power delay product of various Double interconnect

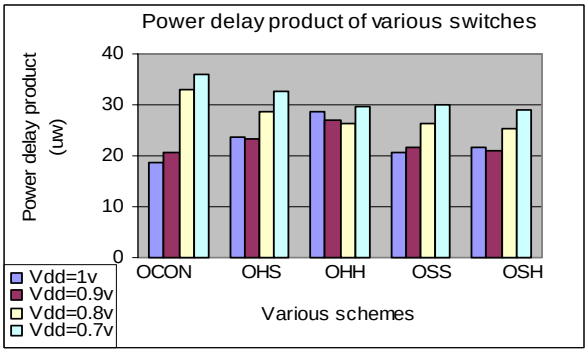

Fig.8 Power delay product of various OMUX interconnect

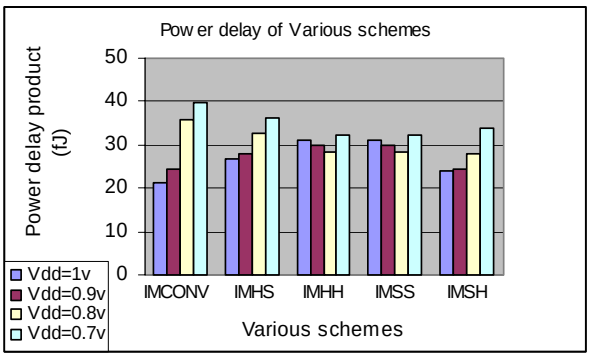

Fig.9 Power delay product of various IMUX interconnect

power delay product (PDP) of simple switches, an average 26.75% improvement in the PDP of Virtex-II interconnect and a marginal improvement in the stand-by leakage.

Since the interconnect fabric of FPGA has thousands of switches (inside the multiplexer and switch box), the overall improvement in PDP for the whole FPGA can be significant. Thus the work described here significantly advances in the state of art low energy FPGA design. The area overhead of the proposed switches and interconnects will be very less if the extra needed transistor for DTMOS based switches is shared intelligently, which is easily possible in all multiplexer based interconnects.

A final complication with DTMOS based switches and interconnects is the process complexity. The isolation to the body contact requires an additional masking step. DTMOS can only be implemented in triple-well process technology. The additional increase in area and process complexities for DTMOS is compensated by its higher operating frequency and higher driving capability as compare to Conventional-CMOS circuit topology. Isolation comes naturally for DTMOS when implemented on SOI wafers but it is quite difficult for the bulk silicon wafers.

VI. REFERENCES

[1] F. Li, D. Chen, L. He, and **J.** Cong, "Architecture evaluation for power-efficient FPGAs," in Proc. ACM Intl. Symp. Field-Programmable Gate Arrays, Feb 2003. pp. 17-21.

[2] Tim Tuan, Bocheng Lai, "Leakage power analysis of a 90nm FPGA" IEEE Custom integrated circuit conference 2003 pp. 57-60.

[3] H. Kim and K. Roy, "Ultra-low power DLMS adaptive filter for hearing aid applications," in *Proc. Int.* Symp. Low Power Electronics and Design, 2001, pp. 352–357.

[4] Xilinx, Inc., Datasheet: Virtex Configuration Guide, September 2000.

[5] Altera, Datasheet: Configuration Devices for SRAM-Based LUT Devices, February2002.

[6] M.Sheng and J.Rose, "Mixing buffers and pass transistors in FPGA routing architectures," in ACM/SIGDA Int. Symp. On FPGA, February 2001, pp. 75- 84

[7] A. Wang, A. P. Chandrakasan, and S. V. Kosonocky, "Optimal supply and threshold scaling for subthreshold CMOS circuits," in *Proc. IEEE* Annu Symp. VLSI, 2002, pp. 5–9.

[8] N. Lindert, T. Sugii, S. Tang and C. Hu, "Dynamic threshold pass-transistor logic for improved delay at lower power supply voltages," IEEE J. Solid-State Circuts, vol.34, no.1,pp.85-90, Jan.1999.

[9] J. Kao, M. Miyazaki, and A. Chandrakasan, "A 175-mV multiply-accumulate unit using an adaptive supply voltage and body bias architecture," IEEE J. Solid-State Circuits, vol. 37, no. 11, pp. 1545–1554, Nov. 2002.

[10] Hendrawan Soleleman and Kaushik Roy, "Robust subthreshold logic for ultra-low power operation," IEEE J. VLSI, vol. 9, no. 1, pp.90-98.

[11] http://www-evice.eecs.berkeley.edu/~bsim3/bism4.html

[12] Betz, **V.,** Rose, J. Cluster-based logic blocks for FPGAs: area-efficiency vs. input sharing and `size` in Proceedings of the IEEE 1997 Custom ntegrated Cir-cuits Conference, May 1997, pp.551-554.

[13] V.Betz, J. Rose, A. Marquardt,"Architecture and CAD for deep-submicron FPGAs," Kluwer Academic Publishers, 1999.

[14] A. Rahman and Vijay Polavarapuv, "Evaluation of low-leakage design techniques for Field Programmable Gate Arrays," FPGA, pp. 23-30, 2004.

[15] L. Shang. A. Kaviani. K. Balhala. "Dynamic Power Consumption in Virtex-II FPGA Family", Proe. of IEEE Symp. on FPGA. 2002.

VII. BIOGRAPHIES

Kureshi A. K. Was born in Ahmendnagar on June 9, 1971. He graduated and post-graduated in electronics engineering from the Pune University. He worked as Asstt. Professor at PDVVP. College of Engineering Ahmednagar. Presently he is pursuing PhD in the department of electronics engineering, Aligarh Muslim University Aligarh. His special field of interest includes low power high speed FPGA design.

Naushad Alam received his B.Tech. degree in Electronics & Communication Engineering in 2003 from Jamia Millia Islamia, New Delhi. He joined as lecturer in Electronics Engineering, University Polytechnic, A.M.U., Aligarh in 2003. Presently he is pursuing M.Tech. in the Electronics Engg. Department, A.M.U. His research interests include Low Power VLSI design, Subthreshold Logic for ultra-low power applications, Network on Chip design etc.

Dr. Mohd. Hasan received the B.Sc. degree in Electronics Engineering in 1990 from A.M.U.,Aligarh. Subsequently, he completed his M.Tech. in Integrated Electronics & Circuits from Indian Institute of Technology, Delhi. He joined as lecturer in the Electronics Engg. Department, A.M.U. in 1992. He became a reader in 1997. He has completed his PhD. in Low Power Architecture for Signal Processing and Telecommunications in the School of Engineering and Electronics, University of Edinburgh, U.K., in 2004. His research interests include low power IC design for wireless communications, and configurable systems on FPGA and so on.