Implementation of FPGA Signal Processing In Software Defined Radios

Ramanna S Havinal and Girish V Attimarad

***Abstract*: FPGA based signal processors are employed in a diverse range of signal processing applications for reasons of performance, economics, flexibility and power consumption. Software defined radios (SDR) are highly configurable hardware platforms that provide the technology for realizing the** rapidly **expanding futuregeneration digital wire less communication infrastructure. Many sophisticated signal processing tasks are performed in a SDR, including advanced compression algorithms, power control, channel estimation, equalization, forward error control, adaptive antennas, rake processing in a WCDMA system and protocol management. Field-programmable gate arrays (FPGA) outpace digital signal processors (DSPs), through hardware execution of a wide range of parallelizable algorithms. FPGAs are especially suited for embedded systems because, beside an area of reconfigurable logical elements, they can also incorporate large amounts of memory, high-speed DSP blocks, clock management circuitry, high-speed input/output (I/O), as well as support for external memory and high speed networking and communications bus standards. Power consumed in embedded systems is very less**

***Index Terms:* Smart Antenna, antenna, Direction of Arrival, FPGA, receiver**

I. INTRODUCTION

TO meet life-style demands we need sophisticated devices to provide voice, high bit-rate data, video, image and multimedia capability. There will also be a range of user terminals that need to be connected to this rich communications tapestry, including cell phones, video phones, satellite phones, PDAs, portable computers and other nomadic computing devices. To flourish and succeed in this dynamic environment we need highly flexible systems that operate across multiple wireless and wired network standards. They must be able to incorporate new signal processing techniques that allow increased network capacity, increased coverage, increased quality of service, or a combination of the above.

Mr. Ramanna S Havinal is Assistant Professor, M.B.E Society's College of Engg, Ambajogai (e-mail: rshavinal@rediffmail.com)
Dr. Girish V Attimarad is Assistant Professor at S D M College of Engig and Tech, Dharwad (e-mail:shreyagiri@rediffmail.com)

The answer to the diverse range of requirements is the *software defined radio*.[7] Software defined radios (SDR) are highly configurable hardware platforms that provide the technology for realizing the future generation digital wireless communication infrastructure. Many sophisticated signal processing tasks are performed in a SDR, including advanced compression algorithms, power control, channel estimation, equalization, forward error control, adaptive antennas, rake processing in a WCDMA (wideband code division multiple access) system and protocol management[2].

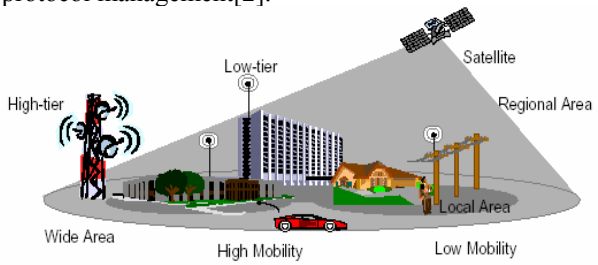

Figure 1: Future generation communication environments will need to support a multitude of modes of operation and air interfaces

For implementing the various functions in a SDR, field programmable gate arrays (FPGAs) are an attractive option for many of these tasks for reasons of performance, power consumption and configurability. This paper will describe how many of the functions required in a software radio system can be realized in an FPGA. The more arithmetically demanding tasks performed in a high data rate wireless system is channel equalization. This paper reviews some hardware implementation of DOA (Direction Of Arrival) The system employs smart antenna, FPGA-based digital signal processor and several analog & digital techniques in RF, IF and digital processing, and can estimate DOAs and do beamforming at very high speed and high accuracy [3][7].

II. FPGA ARCHITECTURE

FPGAs have experienced extensive architectural innovations. Advanced process technology has enabled the development of high density devices that are extremely well suited to the needs to high-performance real-time signal processing. The architecture of the Xilinx Virtex-II is shown in Figure 2. The device is organized as an array of logic elements and programmable routing resources used to provide the

connectivity between the logic elements, FPGA I/O pins and other resources such as on-chip memory, delay lock loops and embedded hardware multipliers[5][7]

The FPGA resources of particular interest to the signal processing engineer are configurable dual-port block memories, distributed memory and the multiplier array [7]. The multiplier array is composed of 18x18-bit precision mutlipliers that can operate in combinatorial mode (140 MHz) or they can be pipelined (1-stage) to support clock frequencies up to 250 MHz. The smallest Virtex-II device provides a modest 4 multipliers while the largest supplies an impressive 192 multipliers.

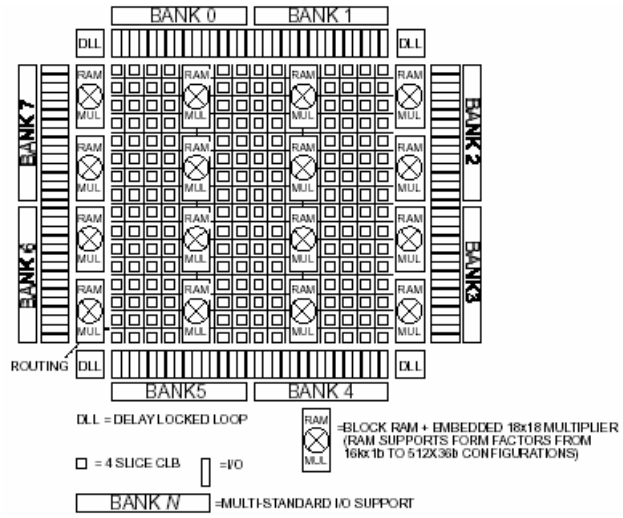

Figure 2: Virtex-II FPGA architecture. This FPGA family provides an array of 18x18-bit precisionmultipliers for addressing advanced sign al processing applications

The FPGA resources of particular interest to the signal processing engineer are configurable dual-port block memories, distributed memory and the multiplier array [6]. The multiplier array is composed of 18x18-bit precision mutlipliers that can operate in combinatorial mode (140 MHz) or they can be pipelined (1-stage) to support clock frequencies up to 250 MHz. The smallest Virtex-II device provides a modest 4 multipliers while the largest supplies an impressive 192 multipliers.

III. SOFTWARE DEFINED RADIOS

The ever-increasing demand for mobile and portable communication requires high-performance systems employing advanced signal processing techniques. These systems must be flexible enough to allow the rapid tracking of evolving and fluid standards. Software defined radios are emerging as a viable solution for meeting the conflicting demands in this arena. SDRs support multimode and multiband modes of operation and are more flexible[3][7]

DSP microprocessors, even with advanced architectural extensions (Very Long Instruction Word (VLIW), super-scalar, etc.) do not satisfy the arithmetic or I/O requirements of a modern communication signal processing engine. Advanced field programmable gate array technology offers a solution. FPGA-based signal processors provide high-performance, while at the same time maintaining flexibility through static RAM configurability [7].A receive subsystem of a concept FPGA-based base transceiver station (BTS) is shown in Figure 3. The figure also shows various feedback loops for providing digital gain control in the digital down converters (DDCs) in addition to a digitally controlled AGC (automatic gain control) loop. Typically this will be a low-bandwidth loop which allows the application of novel sigma-delta modulation techniques[1] for efficiently generating analog signals using FPGAs without the requirement of a digital-to-analog converter (DAC)[4][7].

There are many advanced signal processing tasks performed in a modern digital receiver. Figure 3 illustrates a system consisting of two sub-systems – a front-end high-data rate (100-200 MHz) processor and a back-end symbol rate (or chip-rate in the context of WCDMA) processing fabric.The front-end high-data rate FPGA DSP implements canallization functions for a multi-carrier system. Each channelizer accesses the digital IF , translates a channel (e.g. a 5 MHz wide spectral segment for WCDMA) to base band and using a multi-stage multi-rate filter adjusts the sample rate to satisfy Nyquist for the selected band. The back-end processor will typically operate on multiple slower rate sample streams performing functions like rake processing, adaptive rake processing, demodulation, turbo decoding, Viterbi decoding. In a QAM system, carrier recovery, timing recovery and adaptive channel equalization will be required. The SDR BTS transmitter in Figure 4 implements multiple channels of digital up-conversion, modulation, forward error control, adaptive pre-distortion for high-power amplifier linearization and beam forming for smart antenna,arrays[5][7]

IV. DIRECTION OF ARRIVAL ESTIMATION

Smart antenna system which enables ultra high speed DOA (Direction Of Arrival) estimation and beam forming at reasonable cost is desired for high speed wireless data transmission. Ultra high speed wireless data transmission more than 100 Mbps will be expected in the near future. It is needed to develop an efficient smart antenna system which searches location of mobile terminal and directs a sharp beam to the target direction.Smart antenna is an adaptive antenna system involving spatio temporal baseband signal processing. Unitary MUSIC (MUltiple SIgnal Classi.cation) Processor (UMP) can be used very high speed DOA estimation.[6][7]

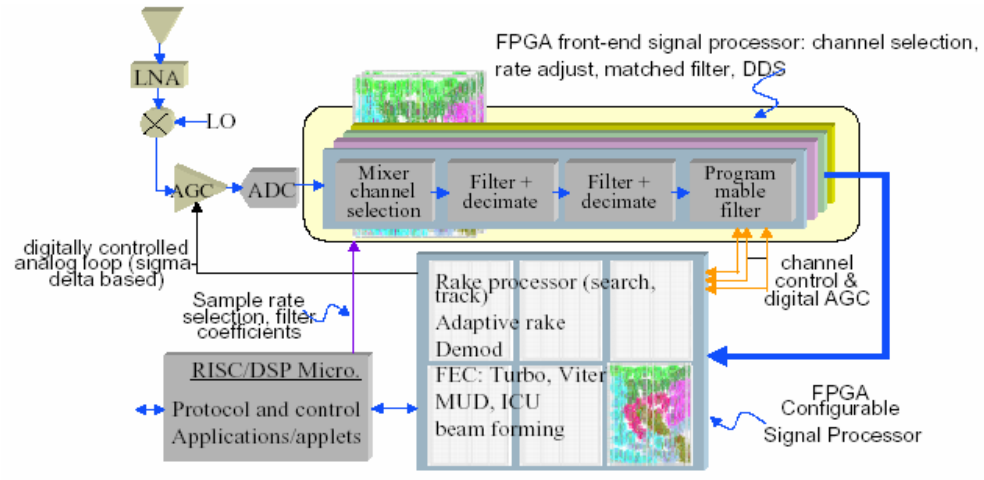

Figure 3: SDR BTS employing FPGA reconfigurable DSP – receiver.

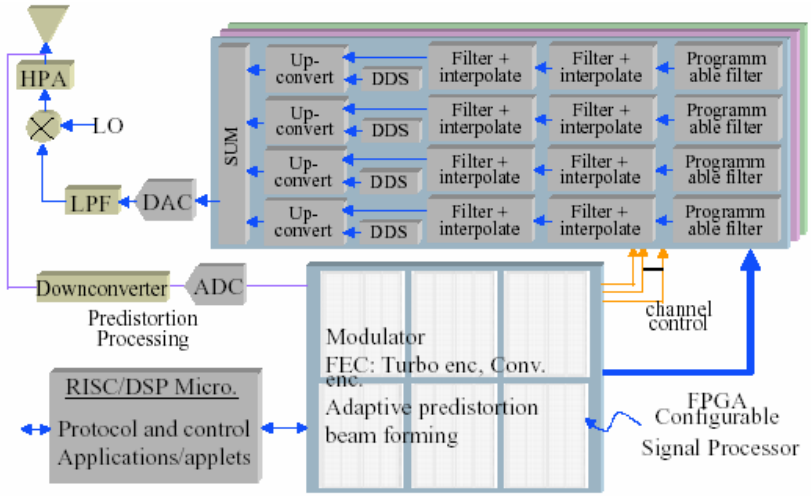

Figure 4: SDR BTS employing FPGA reconfigurable DSP – transmitter

A Fast DOA Estimator by Unitary MUSIC Processor(UMP

Unitary MUSIC Processor (UMP) [3], an FPGA-based DOA estimation system based on Unitary MUSIC algorithm [3].The system can be implementd on 2 FPGAs (EP20K600, Altera) which had about 1.2 million equivalent gates and 80 Kbytes internal memory block totally. The whole block diagram of the DSP procedures is shown in Fig.5. It is involved in 4 major procedure sections including Correlation Matrix Section, EVD Section, FFT Section and LM Detection Section. The bit precision of every section is also shown in this figure. Here we assume that the exact number of waves were predetermined and known in advance from any other process. [6][7][8]

B. UMP Based Beamformer For Eliminating Interferences

A beamforming system based on UMP consists of a DOA estimator and a beamformer as shown in Fig 6. The DOAs of the user signal and interferers are estimated and assumed to be classi.ed properly. It steers the main lobe toward the user direction and totally suppresses the interferers by low side lobe. The performance of the proposed system including DOA estimator and DOA-based beamformer can be evaluated through computer simulations. Assume that four waves including single user and three interferers (two of them are in-beam interferers) arrived at 8-element half-wavelength ULA[6][7][8]

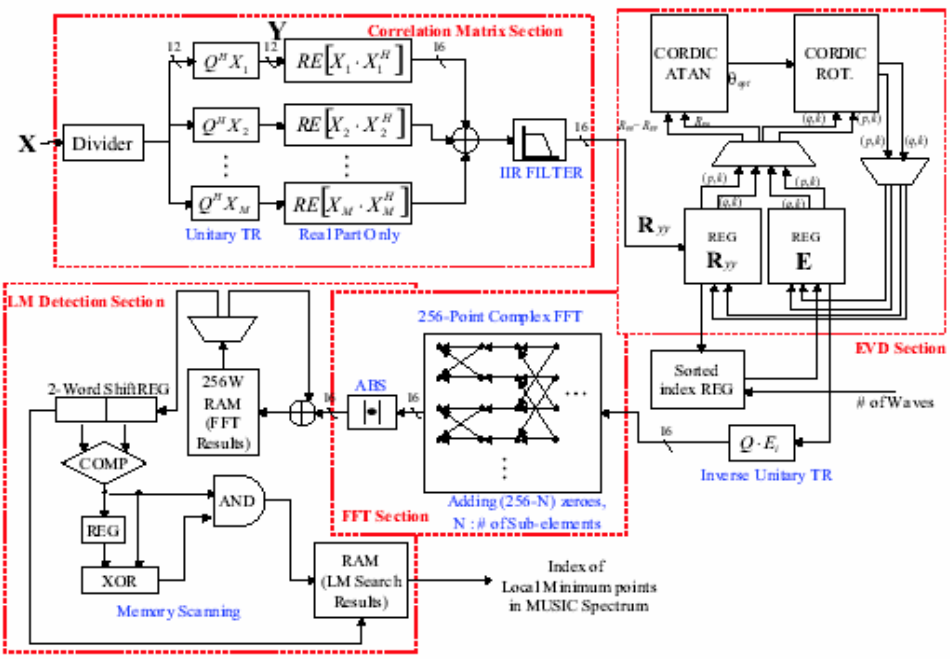

Figure 5: DSP block Diagram

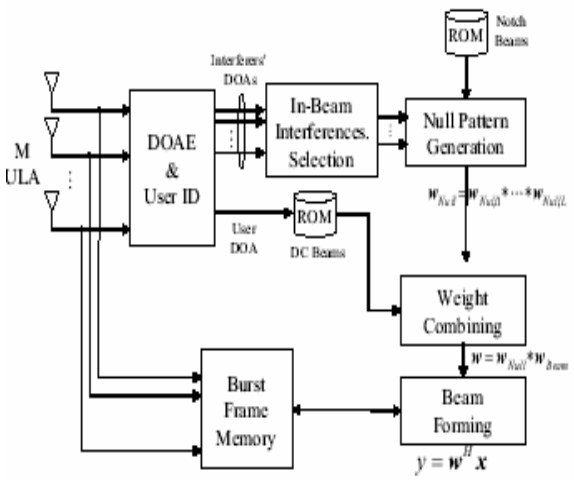

Figure 6: Realtime UMP-Smart Antenna System

V DSP FUNCTIONS IN A DIGITAL RECEIVER

we consider the FPGA implementation of two functions commonly found in many receiver architectures: adaptive channel equalizers and digital down conversion.

A. Channel Equalisers

Most modern bandwidth efficient communication systems use quadrature amplitude modulation. The input data stream is partitioned into sets of *N* bits. These bits are used to select one of 2^N possible waveforms that are both amplitude and phase modulated. The waveforms are each directed to the channel, each with the same shape and bandwidth. Figure 7 shows an equalized receiver[2][7].

Adaptive equalizers operate in a receiver to minimize intersymbol interference (ISI), due to channel-induced distortion, of the received signal. The equalizer operates in cascade with a matched filter (MF), synchronous sampler, and decision device (slicer) operating at the symbol rate. A gradient descent process such as the least-mean square (LMS) algorithm adjusts the equalizer weights to minimize the difference between the input and output of the decision device.[5][6]

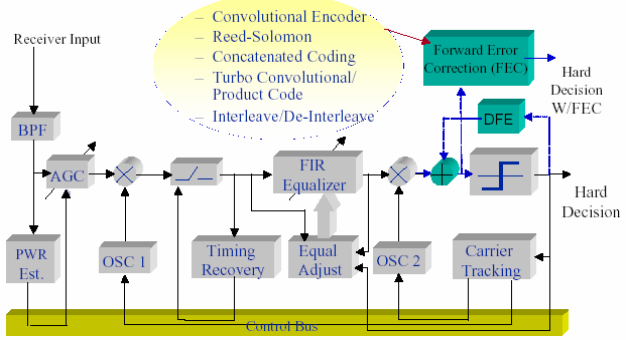

Figure 7: Equalized data demodulator.

In modern receivers the sampling process precedes the matched filter, and in order to satisfy the Nyquist criterion for the matched filter, the sample rate is greater than the symbol rate by a ratio of small integers p-to-q such as 3-to-2 or 4-to-3 and often is 2-to-1 to simplify the subsequent task of down sampling prior to the slicer. If the down sampling occurs prior to the equalizer, the equalizer operates at 1-sample per symbol and it is termed a symbol equalizer, and if the down sampling occurs after the equalizer, the equalizer operates on p/q-samples per symbol and it is termed a fractionally-spaced equalizer (FSE)[2][3][7].

There are also a large number of algorithmic choices for implementing the coefficient update process – least-mean-square, fast Kalman, conventional Kalman, square-root Kalman and recursive-least-square (RLS) lattice to name a few. One of the most successful, because of its simplicity and excellent behavior under finite arithmetic conditions, is the least mean- square algorithm [4][5]. A brief review of the procedure, based on the derivation in [5], follows.The basic adaptive FIR structure is shown in Figure 8. The error signal ε_k can be expressed as

$$\varepsilon_k = d_k - \mathbf{X}_k^{\mathrm{T}}\mathbf{W}_k \qquad (1)$$

where $\mathbf{X}k$ is the regressor vector and the $\mathbf{W}k$ are the filter coefficients. In the LMS algorithm ε^2 is used as an estimate of the gradient on the performance surface [6][8].

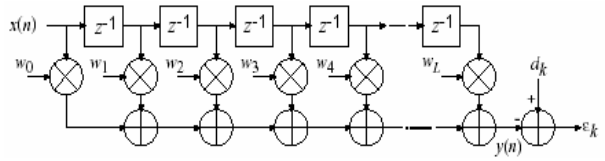

Figure 8: Adaptive transversal filter.

At each iteration in the adaptive process we have a gradient estimate of the form

$$\hat{\nabla}_k = \begin{bmatrix} \frac{\partial \varepsilon_k^2}{\partial w_0} \\ \vdots \\ \frac{\partial \varepsilon_k^2}{\partial w_L} \end{bmatrix} = 2\varepsilon_k \begin{bmatrix} \frac{\partial \varepsilon_k}{\partial w_0} \\ \vdots \\ \frac{\partial \varepsilon_k}{\partial w_L} \end{bmatrix} = -2\varepsilon_k \mathbf{X}_k \qquad (2)$$

With this simple estimate of the gradient we can specify a steepest descent adaptive algorithm that is described by the following equations

$$\begin{aligned} \mathbf{W}_{k+1} &= \mathbf{W}_k - \mu\hat{\nabla}_k \\ &= \mathbf{W}_k - 2\mu\varepsilon_k \mathbf{X}_k \end{aligned} \qquad (3)$$

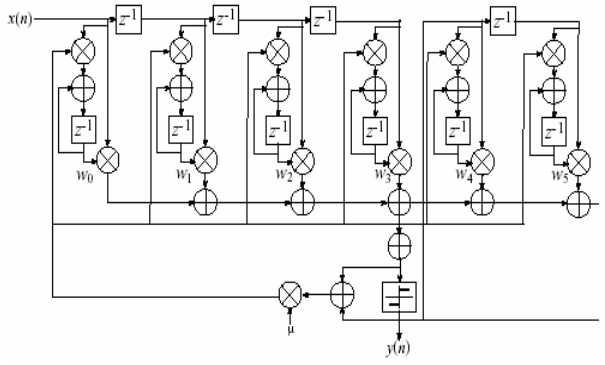

Figure 9: Decision feedback equalizer.

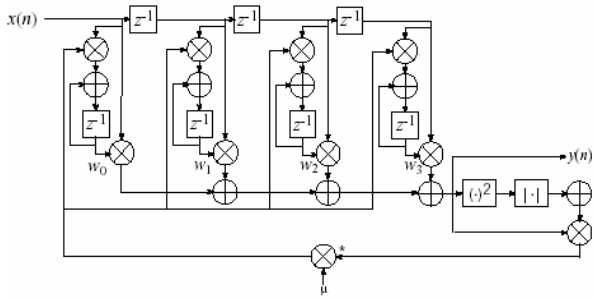

Figure 10: Blind CMA equalizer.

Figures 9 and 10 show a decision feedback and constant modulus algorithm (CMA) blind equalizer respectively. Each equalizer shows the hardware realization of the LMS update algorithm described in Eq. (3).

A fractionally-spaced equalizer can be designed for a Virtex-II FPGA by starting with Matlab floating-point m-file simulations. [5][6]

B. Channelisation

Virtually all digital receivers perform channel access using a digital down-converter (DDC). Modern base station transceivers will often require a large number of DDCs to support multicarrier environments or for coherently down-converting and combining a number of narrow-band channels into one wide-band digital signal. The DDC is typically located at the front-end of the signal processing conditioning chain, close to the A/D, and is usually required to support high sample rate processing in the region of 100 to 200 mega-samples-per-second. The high data rate, coupled with the large arithmetic workload, are not well suited for DSP microprocessor implementation [4][7]. Application specific standard products (ASSP) are a common solution[2].

A more flexible, and typically higher-performance alternative, is to implement the DDC using programmable logic. Since DDC functions only require a modest amount of FPGA silicon resources, many other receiver functions can be implemented in the same device. Consider the implementation of a single channel of the GC4016 quad digital receiver [6][8]. A simplified block diagram is shown in Figure11.

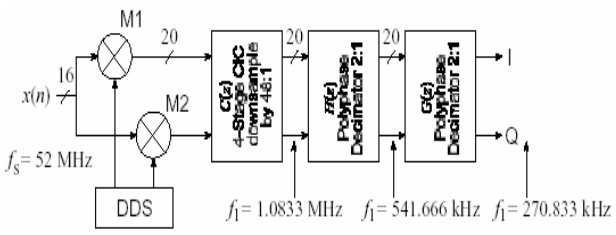

Figure11. Digital down converter architecture.

The desired channel is translated to baseband using the digital mixer comprising the multipliers *M1, M2* and a direct digital synthesizer (DDS). The sample rate of the signal is then adjusted to match the channel bandwidth.This is performed using a multi-stage multi-rate filter consisting of the filters *C(z ,G(z)* and *H(z)*. The functions performed in the system are waveform synthesis (DDS), complex multiplication and multirate filtering[4][5][6].

The multipliers *M1* and *M2* are implemented using the Virtex-II embedded multipliers. Using the optional pipelined mode of operation the embedded Virtex-II multipliers can support samples rates in excess of 200 MHz. In this design, with an input sample rate of 52 MHz, a single multiplier could be time-shared to implement the input heterodyne. The DDS employed is a phase-dithered look-up table-based synthesizer[4]. The FPGA block memory is used to store one quarter of a cycle of a sinusoid. The dual-port memory enables both the in-phase and quadrature components of the local oscillator to be generated simultaneously using a single block RAM. The single block RAM implementation can generate a 4096-sample full-wave 16-bit precision complex sinusoid. With phase dithering, the synthesizer will generate a mixing signal with a spurious free dynamic range (SFDR) of approximately 84 dB. Space constraints inhibit a comprehensive description of the DDS. Details can be found [6][7].

VI CONCLUSION

FPGA based signal processors are being employed in a diverse range of signal processing applications for reasons of performance, economics, flexibility and power consumption. Even though FPGA DSP systems represent a significant faction of the signal processing arena, we are witnessing an exponential growth in the insertion of FPGAs in DSP hardware.Future generation communication infrastructure must support multiple modulation formats and air interface standards. FPGAs provide the flexibility to achieve this goal, while simultaneously providing high levels of performance.The software in a SDR defines the system personality, but currently, the implementation is often a mix of analog hardware, ASICs, FPGAs and DSP software.The rapid uptake of state-of-the-art semi-conductor process technology by FPGA manufacturers is opening-up new opportunities for the effective insertion of FPGAs in the SDR signal conditioning chain. Functions frequently performed by ASICs and DSP processors can now be done by configurable logic. This paper has provided an overview of how several signal processing functions can be implemented in an FPGA.

VII REFERENCES

Periodicals:

[1] Chris Dick and Fred Harris, ``FPGA Signal Processing Using Sigma-Delta Modulation", *IEEESignal Processing Magazine* Vol.17, No1, pp.20-35, Jan 2000.

[2] B. Widrow and S. D. Stearns, *Adaptive Signal Processing*, Prentice Hall, New Jersey, 1985.

[3] C. H. Dick and F. J. Harris, "Direct Digital Synthesis – *Some options for FPGA Implementation*, *SPIE International Symposium on Voice Video and Data Communication,* Boston, Mass., 19- 22 Sept. 1999.

[4] Peled and B. Liu, "A New Hardware Realization of Digital Filters", *IEEE Trans. on Acoust., Speech, Signal Processing*, vol. 22, pp. 456-462, Dec. 1974.

[5] E. B. Hogenauer, "An Economical Class of Digital Filters for Decimation and Interpolation",*IEEE. Trans. Acoust., Speech Signal Processing*,Vol.29,No.2,pp.155-162,April 81.

[6] C. H. Dick and F. J.Harris, "Direct Digital Synthesis - Some Options for FPGA Implementation", *SPIE International Symposium On Voice Video and Data Communication: Reconfigurable Technology: FPGAs for Computing and Applications* Stream, Boston,,USA, pp. 2-10, Sept 20-21 1999.

Technical Reports

[7]Design and Implementation of High-Performance FPGA Signal Processing Datapaths for Software Defined Radios, Chris H. Dick Xilinx Inc.,Henrik M. Pedersen

[8] M. Kim, K. Ichige and H. Arai, "Real-Time Smart Antenna System Incorporating FPGA-Based Fast DOA Estimator," Proc. IEEE Vehicular Technology Conference (VTC 2004-fall), Los Angeles, CA, U.S.A., Sep.2004

VII BIOGRAPHIES

Ramanna S Havinal received the B.E(ECE), M.E(Digital Electronics) degree from Karnataka university Dharwad and Pursuing his Ph.D degree in Microwave Communication. He is currently working as Ass.Prof at M.B.E.Society's College of Engg Ambajogai. His research interests include Digital Signal Processing, Wireless Comminication, VLSI

Dr Girish V Attimarad received the B.E(ECE), M.E(Digital Electronics) degree from Karnataka university Dharwad and obtained his Ph.D degree from Delhi College of Engineering, Delhi. He is currently working as Ass Prof at SDM Society's College of Engg and Tech, Dharwad .His research areas are Digital Signal Processing, Wireless Communication, VLSI Electromagnetics