Computation of Some A/D Converter Parameters Based on Error Estimation using Histogram Test Method

R.S.Gamad, *Member, IETE*, D.K.Mishra, *Member,IEI* and Sunny Gupta

Abstract--**Analog to Digital converter (ADC's) is an important device widely used in many electronics & instrumentation systems for interfacing analog electronics with digital electronics including sensing, video, radar, high speed data acquisition, communication and measurement systems. This paper specially presents the dynamic test methods using Histogram technique for estimation of gain error, offset error, effective number of bit (ENOB) and signal to noise and distortion ratio (SINAD) of ADC with sine wave as input test signal. Code transition levels of ADC transfer characteristics are computed than gain error, offset error, ENOB and SINAD of 5 bit simulated ADC is determined. Here we extended the test algorithm for the estimation of gain error, offset error, ENOB and determine the SINAD using estimated ENOB of Real life ADC. A comparison with previously published work is carried out. The main aim of dynamic testing is to determine functional parameters of an ADC which is responsible for the accuracy, resolution, speed and linearity of the conversion process.**

Index Terms--**Gain Error, Offset Error, ENOB, SINAD, Histogram Method, ADC Testing, Code transition Levels**

I. Introduction

TESTING and characterizing analog to digital converter (ADC) is still a challenging issue for mixed signal device manufacturers and designers, both in terms of time and cost [1]. Generally the goal of such procedure is to verify in a short time whether a given ADC meets its performance requirements. As known, many techniques in the time, frequency and amplitude domains have been proposed for ADC testing [18]. The histogram test is extensively used in the area of ADC testing to obtain their transfer function and consequently several parameters of interest namely, the integral non linearity (INL), differential non linearity (DNL), effective number of bits (ENOB), gain error and offset error, among others. All these parameters attest the capacity of the ADC to perform its intended function. ADCs are rarely used alone, but are often included in more elaborate systems. The performance of the ADCs will affect the performance of the system where it is included and the precision with which the ADC parameters are known is necessary to compute the precision of the final result of the system using it [15]. The authors have extensively worked in determining the precision of estimates of ADC characteristics obtained with the standard histogram test and other ADC test method [2]-[4] [16]. Other authors have also published valuable contributions in this area in estimation of DNL, INL, gain error, offset error and ENOB of ADC [5]-[10][13][14][17][19]-[22] using different input signals. This is a very active field of research.

This paper focus on the ADC gain error, offset error and ENOB which are characteristics that have not received as much study as the other parameters like INL and DNL for instance. We consider the influence of three factors, namely the amplitude of the stimulus signal, the amount of additive noise present in the ADC itself and in the test setup and the number of samples acquired when performing a test. Other factors, like phase noise and frequency error, can also potentially affect the gain and offset error estimates uncertainty but the study of their influence will be relegated for a separate publication [15]. Here we have determined the variance of the ADC gain and offset error estimates and compare our results with earlier methods and we have found better results.

II. Real Life Model of an ADC with Gain error and offset error

An analog signal has infinite possible voltage levels between any two values. But when it is converted in to digital form it contains only limited possible codes depending upon resolution, N, of the ADC (Possible codes = 2N). Fig.1 shows the real life ADC model. If the line does not pass through the origin, it is said that ADC has an offset error and if the angle of the line is not 45 degree then the ADC has gain error. If the

This work has been carried out in SMDP VLSI laboratory of the Electronics and Instrumentation Engineering department of Shri G. S. Institute of Technology and Science, Indore, India. This SMDP VLSI project is funded by Ministry of Information and Communication Technology, Government of India. Authors are thankful to the Ministry for the facilities provided under this project.

R.S.Gamad is with the Department of electronics & instrumentation Engg., Shri G. S. institute of technology and science, 23 Visvesvaraya marg (Park Road) Indore (e-mail: rsgamad@gmail.com)

D.K.Mishra is with the Department of electronics & instrumentation Engg., Shri G. S. institute of technology and science, 23 Visvesvaraya marg (Park Road) Indore (e-mail: mishrak_d@hotmail.com)

Sunny Gupta is with the Department of electronics & instrumentation Engg., Shri G. S. institute of technology and science, 23 Visvesvaraya marg (Park Road) Indore (e-mail: sunnygupta84@gmail.com)

line is not a straight line at all then, ADC has a nonlinearity error. Gain error and offset error present in a practical ADC can be minimized but nonlinearity error can not be reduced unless an ADC with low non-linearity error is selected [3, 5, 19 - 22].

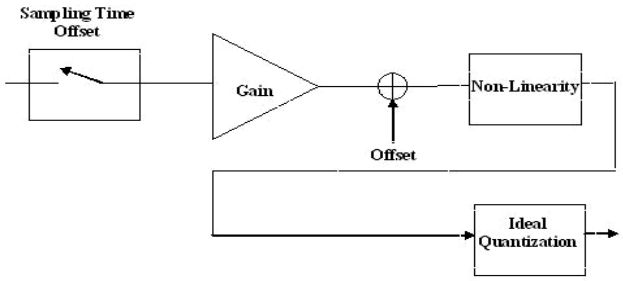


Fig. 1. Real life ADC Model

There are different types of transfer functions. One of them used with bipolar ADCs, represented in Fig.3 and known as "with no true zero". Variable nb represents the ADC number of bits and Fs the full scale voltage.

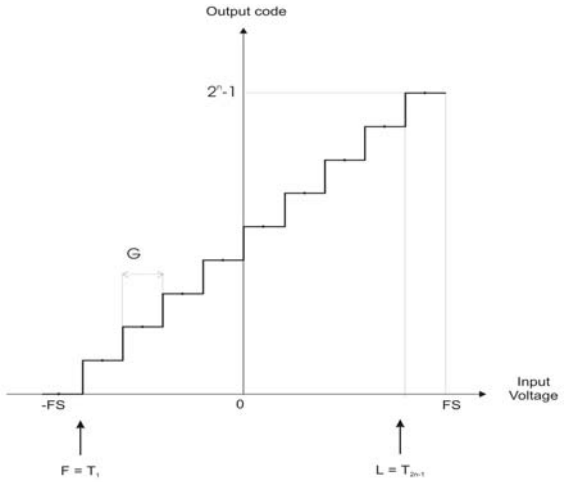


Fig. 2. The transfer function of a bipolar ADC with 'no true zero'.

The transition voltages, T_K, define the ADC transfer function, that is the relation between input voltage and output code, K for an ideal ADC the transition voltages of the transfer function, defined as in fig.2 [15]are

$$T_{K(Ideal)} = -FS + K.Q \quad (1)$$

where, Q = Ideal code bin width, K = Output code, T_K = Transition Voltages.

They are equally spaced by an amount Q given, from the definition of the transfer function by

$$Q = \frac{2\,FS}{2^{nb}} \quad (2)$$

In real life ADC, the real transition voltage will be different from the ideal ones. To express those differences several parameters are used. Two of those are the ADC gain error and offset error. According to the terminal based definition, the offset error plus the product of the gain by the first and last real transition voltages, results in the first and last ideal transition voltages respectively. So that the gain (G) and offset error (O) satisfy the definition if they are computed with the following expressions [15]:

Gain $G = \frac{H_{ideal} - L_{ideal}}{H - L}$ and Offset

$$O = L_{ideal} - GL \quad (3)$$

H = Highest transition voltage, L = Lowest transition voltage

We introduced the variables, $H = T_{2^{nb}-1}$ and L = T_1

When testing an ADC with the (SHT) we obtain an estimate of the transition voltages. From those estimated we can compute the estimated ADC gain error and offset error with software simulation.

$$\hat{G} = \frac{H_{ideal} - L_{ideal}}{\hat{H} - \hat{L}} \quad \text{and} \quad \hat{O} = L_{ideal} - \hat{G}\hat{L} \quad (4)$$

The top hat cover of the symbols signifies that they are an estimative and not the actual values for the ADC under test.

III. ESTIMATION OF GAIN ERROR AND OFFSET ERROR

The terminal based gain and offset error are a function of two random variables, namely the lowest and highest estimated transition voltages $\hat{L}$ and $\hat{H}$. They will also be random variables; we will now determine the standard deviation of the estimated gain and offset error. The variance of the estimated gain and offset error can be approximated by [11, pp. 156]**.** Approximating the mean of the estimated values of $\hat{L}$ and $\hat{H}$ by their ideal values lead to [1]:

$$\sigma_{\hat{G}}^2 \approx \left(\frac{1}{H_{ideal} - L_{ideal}}\right)^2 \sigma_{\hat{L}}^2 + \left(\frac{1}{H_{ideal} - L_{ideal}}\right)^2 \sigma_{\hat{H}}^2 \quad (5)$$

$$\sigma_{\hat{O}}^2 \approx \left(\frac{H_{ideal}}{H_{ideal} - L_{ideal}}\right)^2 \sigma_{\hat{L}}^2 + \left(\frac{L_{ideal}}{H_{ideal} - L_{ideal}}\right)^2 \sigma_{\hat{H}}^2 \quad (6)$$

On a bipolar ADC, with a "no true zero' Transfer function "one has from (1),

$H_{ideal} = -L_{ideal} = FS - Q$

Equation (6) & (7) simplifies to

$$\sigma_{\hat{G}}^2 \approx \frac{1}{4(FS - Q)^2}\left(\sigma_{\hat{L}}^2 + \sigma_{\hat{H}}^2\right) \quad (7)$$

$$\sigma_{\hat{O}}^2 \approx \frac{1}{4}\left(\sigma_{\hat{L}}^2 + \sigma_{\hat{H}}^2\right) \quad (8)$$

Expression (7) & (8) expresses the variance of the estimated gain and offset error as a function of the variance of the first and last estimated transition voltages[15]. The standard Histogram method consists in applying a sinusoidal stimulus signal, with frequency f, amplitude A and offset C, to the ADC under test, and acquiring a predefined number of samples M with sampling frequency fs. The output codes obtained are then grouped into classes forming a histogram, more precisely a cumulative histogram, since the number of elements, Ck, in each class k is the number of samples with output codes equal to or lower than k. From the cumulative Histogram the transition voltages are estimated using [3] [5]

$$\hat{T}_{K+1} = C - A.Cos\left(\pi \frac{C_k}{M}\right) \quad (9)$$

The number of counts in the cumulative Histogram is a random variable. From (9) one can determine the variance of the estimated transition voltages [21, pp. 113],

$$\sigma_{\hat{T}+1}^2 \approx \left(\frac{A\pi}{M}\right)^2\left[1-\left(\frac{T_{K+1}-C}{A}\right)^2\right]\sigma_{C_k}^2 \quad (10)$$

The variance of the number of counts of the cumulative Histogram depends on the real transition voltages (T), additive noise standard deviation (σ) and number of samples(M).

$$U_K = \frac{T_K - C}{A}, \sigma_n = \frac{\sigma}{A} \quad (11)$$

This variance can be represented as a function of the normalized transition voltages (U), normalizes additive noise standard deviation (σ_n), given by (11), and the number of acquired samples (M). Here we are not interested in the maximum value of the variance for all transition voltages but are interested instead on the variance of the number of counts of the cumulative histogram for the first(lowest) and lost (highest) transition voltages. The approximate expression we used here [16] is

$$\sigma_{C_K}^2 \approx Max\left(\frac{1}{4}, \frac{M}{\pi\sqrt{\pi}}\frac{\sigma_n}{\sqrt{1-U_{K+1}^2}}\right) \quad (12)$$

Which is good approximation for practical values of $\sigma_n <$ 0.1

Using (10) & (12) we can derive an approximate expression for the variance of the estimated transition voltages

$$\sigma_{\hat{T}_{K+1}}^2 \approx \left(\frac{A\pi}{M}\right)^2\left(1-U_{K+1}^2\right)Max\left(\frac{1}{4}, \frac{M}{\pi\sqrt{\pi}}\frac{\sigma_n}{\sqrt{1-U_{K+1}^2}}\right) \quad (13)$$

From (7) & (8) considering that for a bipolar ADC with a "no true zero" transfer function, the first (lowest) and last (highest) transition voltages are symmetric and their estimative has the same variance, we can write

$$\sigma_G \approx \frac{\sigma_{\hat{T}[0]}}{\sqrt{2}(FS-Q)} \text{ and } \sigma_{\hat{O}} \approx \frac{\sigma_{\hat{T}[0]}}{\sqrt{2}} \quad (14)$$

Introducing (13) into (14), we have an approximate expression for the variance of the estimated gain and offset error are:

$$\sigma_{\hat{O}} = (FS - Q)\sigma_{\hat{G}} =$$

$$\left(\frac{A\pi}{M}\right)\frac{1}{\sqrt{2}}\left(\sqrt{1-U_O^2}\right)Max\left(\frac{1}{4}, \frac{M}{\pi\sqrt{\pi}}\frac{\sigma_n}{\sqrt{1-U_O^2}}\right) \quad (15)$$

IV. ESTIMATION OF ENOB

The ENOB may be considered as number of bits of a perfect ADC whose rms quantization noise error would be equal to total rms error from all sources in the ADC under test. The ENOB can be expressed as [4] [10] [13] [19]:

$$\text{ENOB} = N - \log_2\left[\frac{\text{rms error (actual)}}{\text{rms error(ideal)}}\right] \quad (16)$$

The rms value of actual and ideal noise can be computed by

$$\text{rms noise (K)} = \left[\frac{\int_{X[K]}^{X[K+1]} e^2\,dx}{x[K+1]-x[K]}\right]^{\frac{1}{2}} \quad (17)$$

Where **e** is the error signal between output and input of transfer characteristic and is expressed as

$$e = p\,x + q \quad (18)$$

equation (22) passes through two points (x(K), e(K)) and (x(K+1), e(K +1)). The parameters p and q can be obtained as

$$p = \frac{e[K]-e[K+1]}{x[K]-x[K+1]} \quad (19)$$

$$q = \frac{1}{2}[e(K) + e(K+1) - p\{x(K) + x(K+1)\}] \quad (20)$$

For ideal case:

$$\mathbf{e}(K) = V_{cbf}(K) - T_b(K) \quad (21a)$$

$$X(K) = T_b(K) \quad (22b)$$

And for actual case:

$$e(K) = V_{cbf}(K) - T(K) \quad (23a)$$

$$X(K) = T(K) \quad (23b)$$

The centre values of best fit transition level V_{cbf} (K) is given by

$$V_{cbf}(K) = \frac{Tb(K+1)+Tb(K)}{2} \quad (24)$$

V. ESTIMATION OF SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists only of quantization noise. As the input frequency increases, the overall noise (particularly in the distortion components) also increases, thereby reducing the ENOB and SINAD. Signal-to-Noise and Distortion Ratio (SINAD) for a full-scale, sinusoidal input waveform is computed [12].

$$SINAD(db) = 6.02 \times ENOB_{estimated} + 1.76 \quad (25)$$

$$\left(S/N\right)_{ideal} = 6.02 \times n + 1.76 \,(\text{db}) \quad (26)$$

VI. RESULTS AND DISCUSSION

In this paper we have tested 5-bit ADC using the histogram test technique with cumulative histogram. And determined the estimated gain error, offset error, ENOB and SINAD using computer simulation technique and verified results with earlier published results. The main results of this paper has expressed by (15), (16) and (25).

A. Gain Error and Offset Error Using Sinusoidal Stimulus Signal

The results for the estimation gain are presented in Table-1 and (Figure3), Table-2 and (Figure 4), Table-3 and (Figure 5) which is better than earlier methods. The variance of the estimated offset error is just scaled version of the variance of the estimated gain, as seen in (7) and (8).

TABLE I
ESTIMATED GAIN AS A FUNCTION OF THE STIMULUS SIGNAL AMPLITUDE

A[v]	$\sigma_{\hat{G}}$ Earlier methods Result	$\sigma_{\hat{G}}$ By our method Result
1.0	0.002	0.00235
1.1	0.00645	0 .0086
1.2	0.0076	0.0095
1.3	0.0084	0.0106
1.4	0.0096	0.021
1.5	0.01	0.023

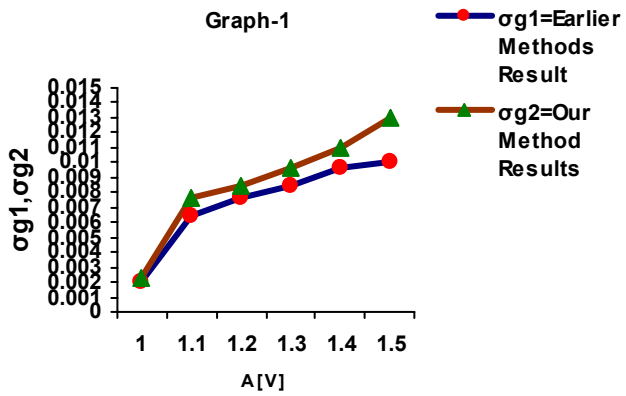


Fig. 3. Estimated gain as a function of the Stimulus Signal Amplitude

TABLE II
ESTIMATED GAIN AS A FUNCTION OF THE NUMBER OF THE SAMPLES

M	$\sigma_{\hat{G}}$ Earlier methods Result	$\sigma_{\hat{G}}$ By our method Result
0	0.0	0.0
200	0.0167	0.016966
400	0.012	0.013934
600	0.0096	0.00988
800	0.008	0.008566
1000	0.0075	0.007634

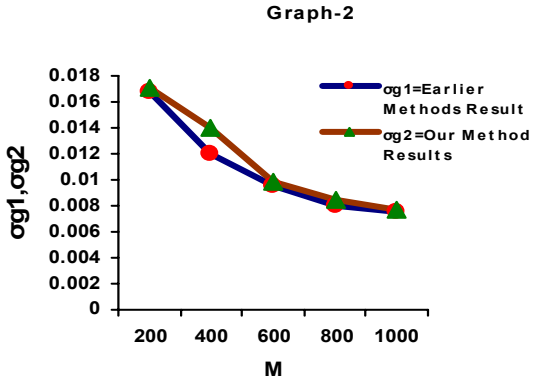


Fig. 4. Estimated gain as a function of the Number of the Samples

TABLE III
Estimated gain as a function of the Normalized Additive Noise Standard Deviation

σ_n	$\sigma_{\hat{G}}$ Earlier methods Result	$\sigma_{\hat{G}}$ By our method Result
0.0	0.0008	0.00087
0.02	0.0036	0.00412
0.04	0.0048	0.00586
0.06	0.006	0.00624
0.08	0.0072	0.00764
0.10	0.00765	0.00889

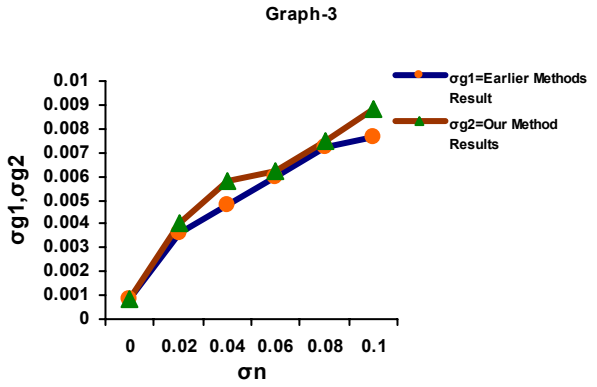


Fig. 5. Estimated gain as a function of the Normalized Additive Noise Standard Deviation

B. *ENOB using Full Scale Sine Wave as Input*

8 bit ideal ADC is simulated and INL error introduced and full scale sine wave of .95 MHZ frequency with peak amplitude (2^{N-1} + 0.5) LSB) (which is sufficient to slightly overdrive the ADC) is sampled by ADC at 5 MHZ frequency. The value of ENOB of an ADC depends on test Conditions such as number of samples, input and sampling frequency. Input and sampling frequency used were not mentioned in the work [7] reported by Wagdy and Awad for ENOB computation. ENOB obtained by our method and earlier method are shown in Table 4. It is clear from Table 4 and Table 5 that results of the method are improved than earlier histogram method [7] for the simulation conditions.

TABLE IV
ENOB Estimation for 5 bit ADC

Number of samples	ENOB by earlier method	ENOB by our method
128	4.342	4.476525
512	4.353	4.498721
1024	4.356	4.536525
2048	4.375	4.537432
4096	4.379	4.548012
8192	4.378	4.561110
11200	4.3757	4.568240
16384	-	4.589201
30000	-	4.593320
31000	-	4.600120
32000	-	4.604501

C. *Signal-to-Noise and Distortion Ratio (**SINAD**) using Full Scale Sine Wave as Input*

The results for SINAD (Using estimated ENOB) are shown in Table 5 and Figure 6.

TABLE V
SINAD for 5 bit ADC using Sine Wave as Input

Number of samples	ENOB by earlier method	ENOB by our method	SINAD Ratio
128	4.342	4.476525	28.708681
512	4.353	4.498721	28.842300
1024	4.356	4.536525	29.069880
2048	4.375	4.537432	29.075341
4096	4.379	4.548012	29.139032
8192	4.378	4.561110	29.217882
11200	4.3757	4.568240	29.260804
16384	-	4.589201	29.386990
30000	-	4.593320	29.411786
31000	-	4.600120	29.452722
32000	-	4.604501	29.479096

$$\left(S/N\right)_{ideal} = 31.86\,db \quad \text{(Exact by (26))}$$

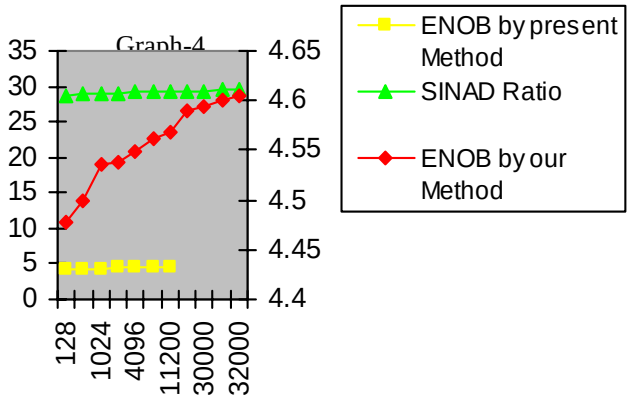


Fig. 6. SINAD for 5 bit ADC

VII. CONCLUSION

In this paper we have determined the precision of the estimates of the ADC gain and offset error obtained with the cumulative histogram method. The main results of this paper can be used to determine the expanded uncertainty, and corresponding uncertainty interval, for the estimated gain and offset error. Here we also compute the ENOB using full scale sine as input stimuli and using this result we have determined the SINAD. Simulation of 5 bit ADC is done and estimate of gain and offset error is determined using cumulative histogram technique and ENOB by our proposed method. There is improvement in estimation using proposed technique as compared to existing technique.

VIII. ACKNOWLEDGEMENT

This work has been carried out in SMDP VLSI laboratory of the Electronics and Instrumentation Engineering department of Shri G. S. Institute of Technology and Science, Indore, India. This SMDP VLSI project is funded by Ministry of Information and Communication Technology, Government of India. Authors are thankful to the Ministry for the facilities provided under this project.

IX. REFERENCES

Periodicals:

[1] Fabrizio stefani, David Macii, Antonio Moschitta, Paolo Carbone and Dario Petri, 'Simple and time effective procedure for ADC INL estimation' *IEEE transaction on instrumentation and measurement,* vol 55, No 4, August 2006.

[2] F.correa Alegria and A.Cruz serra, Influence of Frequency errors in the variance of the cumulative histogram, *IEEE Transaction on Instrumentation and measurements,* vol.50, pp 69-74, Feb 2003.

[3] Francisco Andre correa Algeria and Antonio Manuel da Cruz serra, Variance of Cumulative histogram of ADC's due to frequency errors, *IEEE transaction on Instrumentation and measurement,* vol 52, No 1, Feb 2003.

[4] Jerome Blair, Histogram measurement of ADC nonlinearity using sine waves, IEEE transaction on instrumentation and measurement, Vol 43, no 3, PP 378-383, June 1994.

[5] Fransisco Andre correa Alegria And Antonio Manuel da cruz serra, Overdrive in the ramp Histogram test ADC's, *IEEE transaction on instrumentation and measurement,* vol.54 ,No 6, Feb 2005.

[6] H Koff & K Schon, Digitization errors of fast digital recorders, *IEEE Transaction on Instrumentation and measurement,* Vol IM-36, no-2, pp-423- 427, June 1998.

[7] M F Wagdy & Selim Awad, Determining ADC effective number of bits via Histogram testing, *IEEE transaction on instrumentation and measurement,* vol 40, no 4, august 1991.

[8] D. K. Mishra, N S Chaudhary & M C Shrivastava, New dynamic test methods for determination of Nonlinearity and effective resolution of A/D converters, *IETE journal of research (INDIA),* Vol. 43, no 6 , pp 403-409, Nov - Dec.1997.

[9] D. K. Mishra, ADC testing using interpolated Fast Fourier transforms (IFFT) technique, International *Journal of Electronics, Taylor And Francis,* Vol.90, no *7, PP* 459-469, 2003.

[10] D K Mishra, Dynamic testing of high speed A/D converters using triangular Wave as input test signal, *IE (I) Journal - ET-2005,*Vol 85, pp 68-71, January 2005.

Books:

[11] Athanasios Papoulis, "Probability, Random Variables and Stochastic Process," McGraw-Hill, Third edition, 1991.

[12] Phillip E. Allen and Douglas R. Holberg "CMOS Analog Circuit Design" Oxford, Second edition 2007.

Papers Presented at Conferences (Unpublished):

[13] D. K. Mishra and R. S. Gamad, "Determination of non linearity and effective resolution of an A/D converter for arbitrary application input" proc. of *international conference on circuits and systems,* San Francisco, USA 24-26, OCT. 2007.

Papers from Conference Proceedings (Published):

[14] D. K. Mishra and R. S.Gamad, "Determination of Gain error & Offset error using Histogram Technique" International conf. on soft computing & intelligent systems, ICSCIS-07, JBP India. Vol 2, pp-186-191.

[15] F.Correa Algeria and A.Cruz Serra, 'Precision of ADC gain and offset error estimation with the standard histogram test' *IEEE IMTC 2005 instrumentation and measurement technology conference* Ottawa, Canada 17-19 May 2005.

[16] F.correa Alegria and A.Cruz serra, Uncertainty in the ADC Transition Voltages Determined with the Histogram Method, *Proc. of 6th Workshop on ADC Modeling and Testing,* Lisboa, Portugal, Sept 13-14, pp 28-32, 2001.

Dissertations:

[17] D. K. Mishra, "Some Methods for Dynamic Testing of A/D Converters" Ph. D. Thesis, May 2000.

Standards:

[18] T.E.Linnenbrink, S.J.Tilden and M.T.Miller, 'ADC testing with IEEE std. 1241-2000' in *proc. IEEE IMTC* May 2001 pp 1986-1991.

[19] IEEE–std–1057-1994 (R- 2001), Digitizing waveform recorders, *IEEE Instrumentation and measurement transaction.*2000.

[20] Sergio Rapuano, Pasqute Dponte , Eulalia balestrier Luca devito, stven J . Tilden, Solman max & Terome Blair, ADC parameter and characteristic, *IEEE std 1241-2000(P-6) magazine* April 2006.

[21] Thomas E. linnenbrink , Jerome Blair , Sergio rapuano, pasquale Daponte, Eulalia Balestrieri ,luca de vito , soloman max and steven J .Tilden , ADC testing, *IEEE – std-1241(P-7) instrumentation and measurement magazine* ,APRIL 2005.

[22] 'IEEE std-1241-2000 (p-5) analog to digital conversion, David A. Rauth and vincint T. Randal, *IEEE instrumentation and Measurement magazine* oct 2005.

X. BIOGRAPHIES

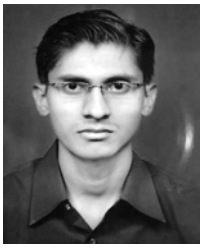
R.S.Gamad was born in Ratlam in India, on 30 Dec, 1970. He Graduated from Govt. Engg. College, Ujjain, India.

He is currently working as a Reader, Electronics and Instrumentation Dept., in Shri G. S. Institue of Technology and Science, Indore, India. His field of research includes Characterization of ADC, VLSI Design and Testing, Communication.

R.S.Gamad received honorary degree from Technical University RGPV, Bhopal, India

Dr. D.K.Mishra was born in India. He Completed his Graduation in 1979 in Electronics Engg. He is currently working as a professor and head, Electronics and Instrumentation Dept., in Shri G. S. Institue of Technology and Science, Indore, India. His field of Research includes Dynamic Testing of A/D, Mixed Signal, BIST for ADC, VLSI Design, FPAA. Dr. D. K. Mishra completed his ME in Applied Electronics and Servomechanism in 1984 and Awarded with Ph.D in Electronics and

Telecommunication in 2000.



Sunny Gupta was born in Meerut in India, on June 29, 1984. He graduated from the Sri Ram Institute of Technology , Jabalpur. His special fields of interest included ADC Designing and Testing. Sunny pursuing M.Tech degree from Shri G. S. Institute of Technology and Science, Indore, India