Modeling of High Temperature Rapid Thermal Oxidation Used in Microelectronic Applications

S. S. Mane, *Member IEEE* and S. S. Rathod, *Member IEEE*

Abstract-- **In the past few years, Rapid Thermal Oxidation (RTO) have gained acceptance as mainstream technology for semi-conductors manufacturing. These processes are characterized by a single wafer processing with a very fast ramp heating of the silicon wafer. The single wafer approach allows for faster wafer processing and better control of process parameters on the wafer. As feature sizes become smaller, and wafer uniformity demands become more stringent, there is an increased demand from rapid thermal (RT) equipment manufacturers to improve control, uniformity and repeatability of processes on wafers. In RT processes, the main control problem is that of temperature, which is complicated due to the high non-linearity of the heating process, process parameters that change significantly during a single wafer process and between processes, and difficulties in measuring temperature and edge effects. The work carried out by extracting the sample data published, we developed our own model for rapid thermal oxidation rate using Deal-Groove model by adjusting the suitable error function. This new model is designed to ensure uniform oxidation rate that varies for different temperatures. The model involves the reverse engineering of the required linear coefficient used in Deal-Groove model. The model for rapid thermal oxidation is implemented in 1-D Process-Wizard and further applied to 2-D SILVACO-ATHENA and verified the improvement in device characteristics of MOSFET. This model can be used safely in the predication of oxidation rate of silicon wafer carried out at 1050^0C to 1250^0C.**

Index Terms-- **MOSFET, Process-Wizard, SILVACO-ATHENA, Rapid Thermal (RT). Rapid Thermal Annealing (RTA), Rapid Thermal Chemical Vapor Deposition (RTCVD), Rapid Thermal Nitration (RTN) and Rapid Thermal Oxidation (RTO).**

I. Introduction

INTEGRATED circuits are at the heart of all electrical appliances. These are based mainly on semiconductor devices, which are fabricated in a sequence of batch chemical processes such as chemical vapor diffusion (CVD), oxidation, nitration, ion implantation, and annealing. Incremental improvements in integrated circuit technology, together with increased performance demands from semiconductor devices, have gradually led to requirements that the variation in the key quality variables be reduced and to the increased yields afforded by larger diameter silicon wafers. This in turn has increased the reliance of the microelectronics industry on advanced process control (APC) strategies, and to seek new fabrication methods. Thermal processes play an important role in the fabrication of semiconductor chips in the microelectronics industry. Shrinking device dimensions to the sub-micron range make stringent demands on the thermal processing of semiconductor wafers. The wafer should spend the minimal time close to the process temperature to reduce the solid-state diffusion of dopants introduced in the previous fabrication steps. The drive to reduce this “thermal budget” and the tight quality demands gave birth to a new technology: single wafer processing (SWP). SWP systems must heat up and cool down quickly in order to compete economically with multi-wafer technology, and this has led to the development of rapid thermal processing (RTP).

RTP involves the processing of single silicon wafers, and is used for various processes for the manufacture of semiconductor devices, such as rapid thermal annealing (RTA), rapid thermal oxidation (RTO), rapid thermal chemical vapor deposition (RTCVD) and rapid thermal nitration (RTN) [1]. A typical RTP operating cycle consists of three phases: (1) rapid heating to the desired operating temperature, (2) the processing phase, in which temperature is held constant, and (3) rapid cooling to ambient conditions. The drive to reduce the “thermal budget” makes RTP an attractive alternative to conventional methods of thermal processing. This goal forces a stiff constraint on the control of the process temperature and thickness uniformity.

As feature sizes become smaller, and wafer uniformity demands become more stringent, there is an increased demand from rapid thermal (RT) equipment manufacturers to improve control, uniformity and repeatability of processes on wafers. In RT processes, the main control problem is that of temperature regulation, which is complicated due to the high non-linearity of the heating process, process parameters that change significantly during a single wafer process and between processes, and difficulties in measuring temperature and edge effects. The rapid heating is made possible using clusters of high powered lamps, with the lamp configuration defining the structure of the RTP system, and the number of pyrometers or other temperature measuring techniques defining the character of the control configuration that can be

S. S. Mane is with Department of Electronics Engineering at Sardar Patel Institute of Technology, Mumbai 400058 INDIA.
(e-mail: ssmane.iitkgp@gmail.com).

S. S. Rathod is with Department of Electronics Engineering at Sardar Patel Institute of Technology, Mumbai 400058 INDIA.
(e-mail: rathod_spce@yahoo.com).

implemented on the RTP system.

Rapid thermal oxidation of silicon has been carried out [1] in the temperature range 1000 to 1250°C for an oxidation time of 5 to 60 sec. The new kinetics data show that oxidation is carried out by a two-energy activation process. Assuming linear growth during the first 5 sec of fast oxidation, the first process occurs with activation energy *Ea* of 0.9eV. The second process takes place with *Ea* of 1.4eV for linear growth kinetics from 5 to 60 sec.

In this paper we developed our own model for rapid thermal oxidation by extracting the published sample data. The available Deal-Groove [3] is applicable for the thermal oxidation of silicon up to the temperature 1050^0C. The oxidation rate estimated by Deal-Groove model differ the actual oxidation rate at temperatures above 1050^0C in case of rapid thermal oxidation. We have modified the Deal-Groove model by adjusting the suitable error function in terms of temperature and linear rate constant (B/A). The model involves the reverse engineering of the required linear coefficient (B/A) used in Deal-Groove model. The proposed model for rapid thermal oxidation is implemented in 1-D Process-Wizard tool and it is further applied to 2-D Silvaco-ATHENA and found the improvement in device characteristics of MOSFET.

II. SIMULATION METHODOLY OF PROPOSED RAPID THERMAL OXIDATION MODEL

The simulations are carried out using the reported experimental data of Rapid Thermal Oxidation of Silicon carried out at the temperature range 1050^0C to 1250^0C [1,2].

A. Extraction of Rapid Thermal Oxidation data

The Rapid Thermal Oxidation is carried out at the temperature range of 1050^0C to 1250^0C. The reported experimental data is extracted from the reference [1,2]. The experimental data i.e. Oxide thickness verses the Oxidation time. These data for the various temperatures is plotted in the Matlab tool. The plotted Oxidation Rate is then compared with the Oxidation Rate predicted by the Deal-Groove Model. The Error obtained between the experimental data and the Deal-Groove model is plotted for the different reported data as shown in fig 1.

B. Kinetics of Rapid Thermal Oxidation

As the Rapid thermal oxidation process is the less time process, it follows the linear rate constant (B/A). The linear rate constant (B/A) is calculated for different reported temperatures by the equation

Besides Deal and Grove's [3] theory of Si-oxidation, several other models have been reported like Massoud et al. [4] and Kageshima et al [5,6], which fit very well with the experimental data, whilst no such specific model has been reported for high temperature oxidation of Silicon so far. In this paper, we report on the development of RTO oxidation model and possible application in TCAD simulations.

The proposed oxidation rate for Silicon is given by the equation (1) below,

$$\frac{dx_o}{dt} = \frac{B}{(A + 2x_o)} + erf(x_o, T) \qquad (1)$$

The above equation consists of two terms,

a) The first term is a linear-parabolic relationship according to the Deal-Grove model of the oxidation kinetics.
b) Whereas, the second term (our modification) contains the error function in terms of error in the reported data and the Deal-Groove model and temperature, where, x_0 is oxide thickness and t_0 (kept 10 nm) is the length of oxidation.

The linear rate constant is then plotted with the reported temperature range from 1050^0C to 1250^0C. And it is found that the linear rate constant (B/A) with respect to temperature is almost the linear in nature. The linear rate constants of the RTO other than the reported data can be extracted with linear curve fit equation of the graph as shown in figure 2. The calculated values of the linear rate constant (B/A) for the various temperatures is shown in the table 1 below.

TABLE I
THE CALCULATED VALUES OF THE LINEAR RATE CONSTANT (B/A) EXTRACTED WITH THE DEAL-GROOVE MODEL.

Temperature in Degree Centigrade	Linear Rate Constant (B/A) in (nm/s)
1050	0.0652
1100	0.138
1150	0.211
1200	0.284
1250	0.375

C. Verification of the Model with Process-Wizard-1D

The Rapid Thermal Oxidation model we proposed is verified with the Process Wizard-1D, which is basically used for the semiconductor process engineering, as it is an easy-to-use and highly accurate tool for simulating the entire Si process flow [9].

For this, the Oxidation of the Silicon wafer is carried out at 1200^0C for 30 Seconds and observed the Oxidation Rate. And we found our Rapid Thermal Oxidation Model fits well with the observed Oxidation Rate.

D. Implementation of the RTO Model in Silvaco-ATHENA

The Silvaco-ATHENA process-to-device simulation is carried out to study the usefulness of our proposed model in TCAD of the Silicon n-MOSFET. The Silvaco-ATHENA simulator [10] also describes the oxidation model almost same to that of the model suggested by the Massoud [4, 10] as shown in equation 2 below,

$$R_{th} = Th_0 \exp(-\frac{Th_E}{kT}) \exp(\frac{X_0}{Th_L}) \qquad (2)$$

Where, Th_0 =18 μm^2 /min, Th_E =2.37eV for <100> orientation and Th_L =0.0069 μm

The value of the parabolic constant [7, 8, 11] is given by,

$$B = C_1 e^{-\frac{E_1}{kT}} = 3.57\text{x}10^{-4} \ \mu\text{m}^2/\text{hr} \quad (3)$$

And the value of the linear rate constant [7, 8, 11] is given by

$$\frac{B}{A} = C_2 e^{-\frac{E_2}{kT}} = 1.28\text{x}10^{-4} \ \mu\text{m/hr} \quad (4)$$

For thin oxide [7, 8], E_1 =1.23 eV, C_1 = 7.72x10^{-2} μm^2/hr, E_2 =2.0 eV & C_2 = 6.23x10^{-6} μm/hr.

Therefore, by calculating all the values from above equations and substituting in the oxidation module of Silvaco-ATHENA we simulate the n-MOSFET structure. The dominant characteristics of the device we made with our oxidation model are observed and found that our Rapid Thermal Oxidation model for Silicon gives better driving current for a given set of V_{DS} and V_{GS} compared to the default oxidation model used in the Silvaco-ATHENA tool as shown in Fig.5 and 6.

III. RESULTS AND DISCUSSION

The error between oxide thickness of the published result [1, 2] and the Deal-Groove model for different oxidation time from 10 sec to 60 sec is plotted against temperatures and is as shown in fig. 1. The Error obtained with respect to temperature for various times from 10 sec to 60 sec is found linear.

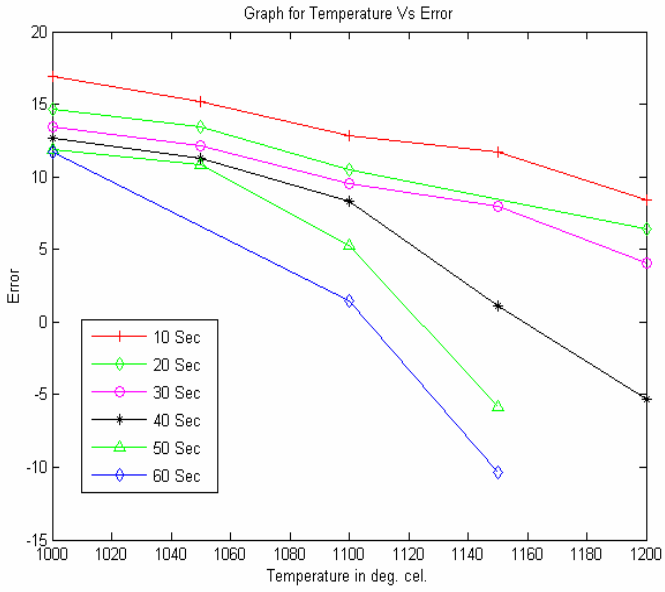

Fig. 1. Plot of Error in Oxidation Rate and Temperature

The linear rate constant (B/A) for different temperatures is plotted in fig. 2. The linear rate constant (B/A) found linear with respect to temperature. The B/A constant for the temperature other than the published data can be extracted from the curve fit equation. The B/A constant for the temperature 1050^{0}C to 1250^{0}C are given in the table 1. Figure 3 show the oxidation rate at different temperatures and it is found that the published data matches the proposed RTO model.

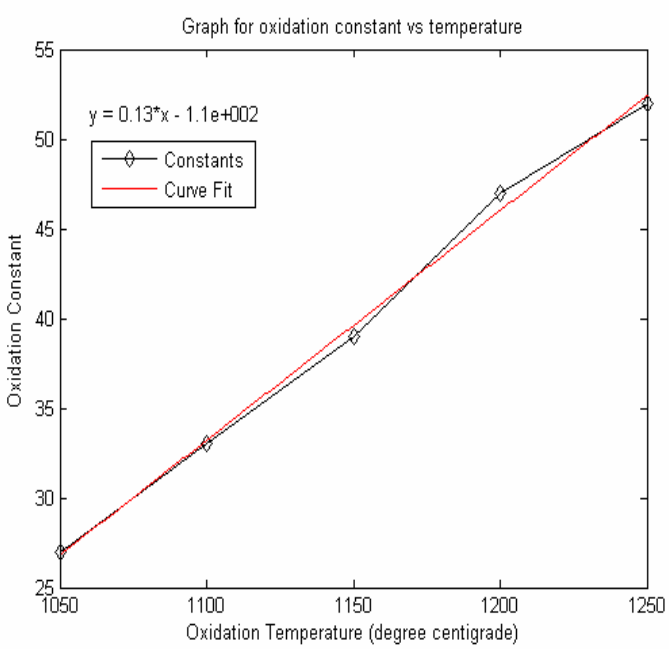

Fig. 2. Plot of Linear Rate Constant (B/A) and Temperature

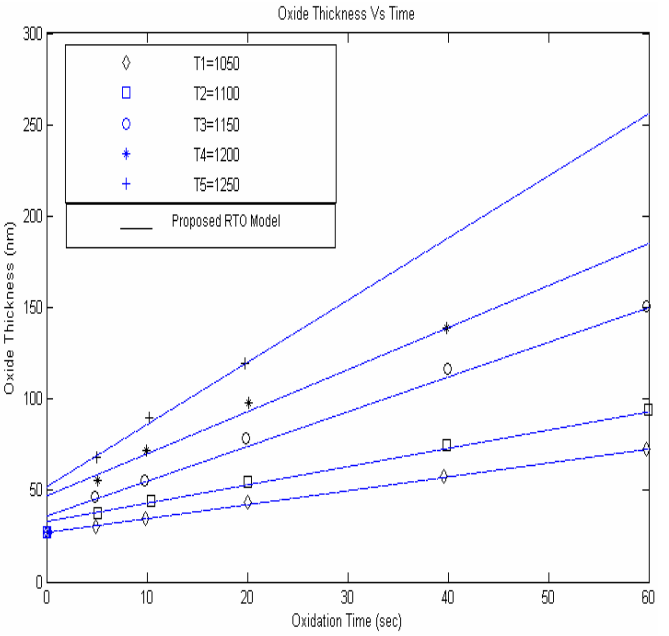

Fig. 3. Plot of Oxide Thickness and Oxidation Time for different temperature for published data and proposed model

The proposed oxidation model is implemented in 1-D process wizard that is used for complete silicon process flow and found suitable for RTO compared to Deal-Groove model for the temperature above 1050^{0}C. The matched parameters of the oxidation model of Silvaco-Athena are modified with our proposed RTO model to grow a thin gate oxide (<10nm).

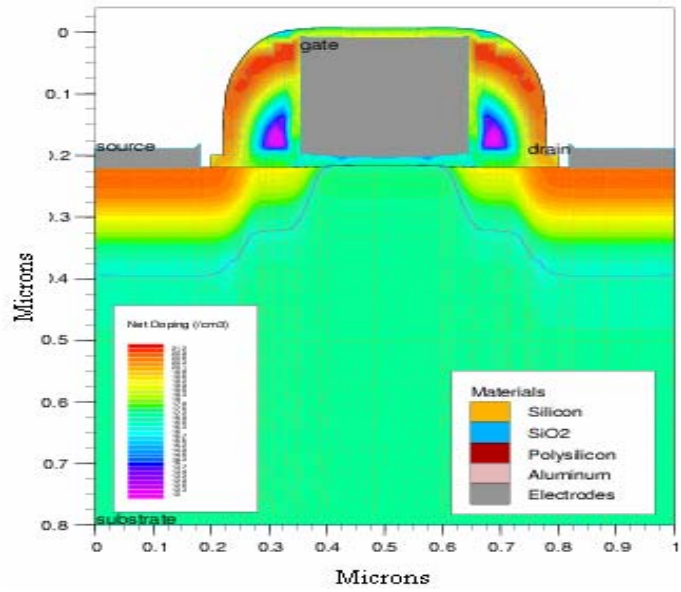

Fig. 4. Device structure of MOSFET after implementation of proposed RTO model developed

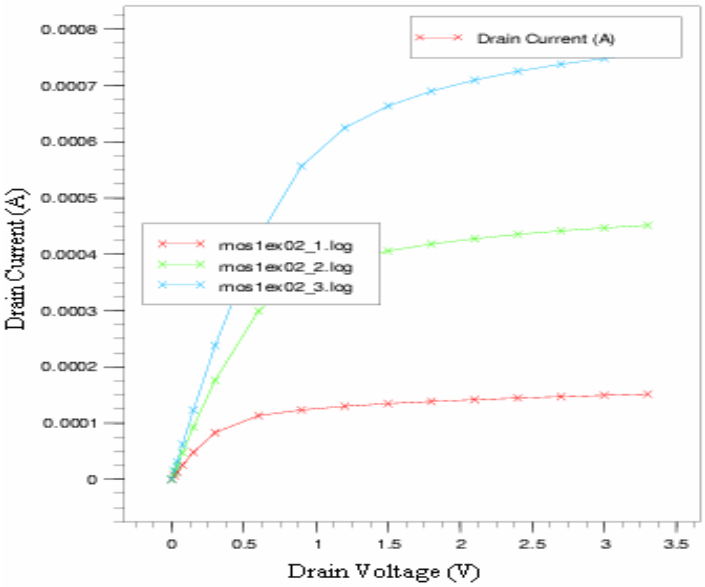

Fig. 6. Plot of I_d-V_d Characteristics of n-MOSFET with proposed RTO model developed after this study

The developed device structure of n-MOSFET after implementation of proposed RTO model is as shown in fig. 4. The developed device (0.2µm) consists of 10nm thin gate oxide. The device characteristics of the n-MOSFET before and after implementation of the proposed RTO model are studied and found the improvement in drain current. The drain current obtained with the default oxidation model used in Silvaco-Athena is observed 0.5mA for the V_{GS} equal to 0.2V while drain current obtained with the proposed model is observed 0.7mA for the same value of $V_{GS.}$ The I_d-V_d characteristics of n-MOSFET with default oxidation model and proposed oxidation model is shown in fig 5 and fig. 6.

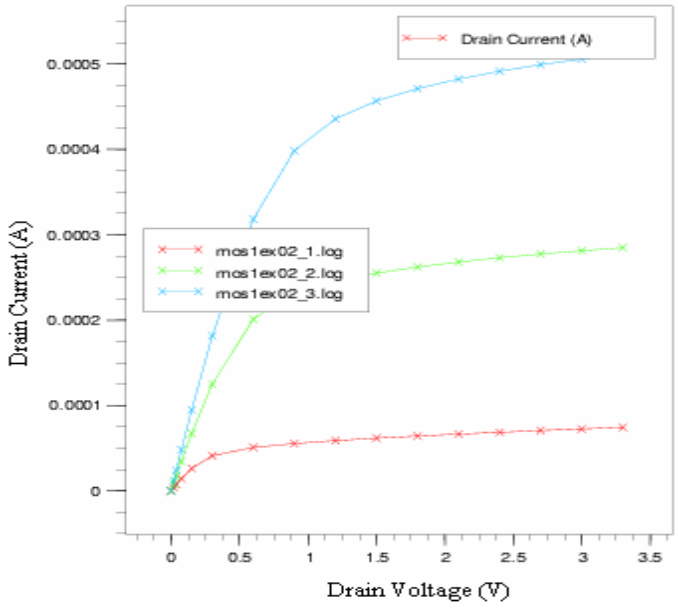

Fig. 5. Plot of I_d-V_d Characteristics of n-MOSFET with default oxidation model used in Silvaco-Athena

IV. Conclusions

We report on the development of simple Rapid Thermal Oxidation model for Silicon for thin oxides grown at high temperatures. Deal-Grove model has been modified via analytical expressions to model thin oxides. The oxidation model uses an additional error function in terms of oxide thickness and temperature. B and B/A coefficients have been extracted from experimental data for high temperature oxidation of Silicon wafer. The model has been verified with the Process Wizard 1D and also implemented in Silvaco-ATHENA Tool for Silicon process simulation, and found that our oxidation model fits well with the reported data. The proposed model may find possible applications in process simulation for Silicon-technology (TCAD).

V. Acknowledgment

The authors gratefully acknowledge the facilities provided in VLSI Laboratory of Electronics Engineering Department, Sardar Patel Institute of Technology, Mumbai.

VI. References

Periodicals:

[1] N. Chan Tung and Y. Caratini, "Rapid themal oxidation of silicon for thin gate dielectric," *IEEE Electronic Letters, Semiconductor Devices and Materials*, vol. 22, No. 13, pp. 694-696, June. 1986.

[2] A. Maury, S. C. Kim, A. Manocha, K. H. Oh, D. Kostelnick and S. Shive, "Application of rapid thermal oxidation to the development of high dielectric strength polyoxides", IEDM, p.p. 676-679, 1986

[3] B. E. Deal and A. S. Grove, "General Relationship for thermal Oxidation of Silicon", J. Appl. Phys. Vol. 36, p.p. 3770-3774, 1965.

[4] H. Z. Massoud, J. D. Plummer, and E. A. Irene, "Thermal Oxidation of Silicon in Dry Oxygen: Accurate determination of kinetic constants", J. Electrochem. Soc., 132 , 2685, 1985

[5] H. Kageshima, K. Shiraishi, and M. Uematsu, “Universal Theory of Silicon Oxidation Rate and Importance of Interfacial Silicon Emission”, Jpn. J. Appl. Phys., 38, L971, 1999.
[6] Uematsu, H. Kageshima, and K. Shiraishi, “Microscopic Mechanism of Thermal Silicon Oxide Growth”, Comp. Mat. Sci., 229, 24, 2002.

Books:

[7] S.M. Sze, “VLSI Technology”, vol. I., 2nd ed, New York: McGraw Hill, 2002, p. 98-138.
[8] S. B. Ghandhi, "VLSI fabrication principles," 2nd ed., New York: Wiley, 2003, pp. 452-508.

Technical Reports:

[9] “Process Wizard – 1D”, Version 1.3, Dawn Technologies, Inc., 1999.
[10] “ATHENA User’s Manual”, Silvaco International, USA

Papers from Conference/Journal Proceedings (Published):

[11] S. S. Mane, S. Hameed, A.R. Saha and C.K. Maiti, "Modeling of Low Temperature SiGe Oxidation," *Elsevier Journal of “Material Science in Semiconductor Processing*, Vol-9, pp. 668-672, Aug-*Oct-2006*

VII. BIOGRAPHIES

S. S. Mane (M’2007) was born in Sangli in India on April 1, 1976. He graduated from the Walchand College of Engineering Sangli, and completed his post graduation in the field of Microelectronics and VLSI Design from Indian Institute of Technology, Kharagpur-India.

His employment experience includes eight years as an educationalist. His special fields of interest include process and device modeling. He received endowment scholarship from APLAB INDIA LTD for his project on control systems. He is member of IEEE, ISTE and ISNT.

S. S. Rathod (M’2007) was born in Amravati in India on Feb 28, 1975. He graduated from the College of Engineering Badnera, and completed his post graduation in the field of Electronics Engineering from V.J.T.I., Mumbai-India. Currently he is pursuing his doctoral research at Indian Institute of Technology, Roorkee-India.

His employment experience includes eight years as an educationalist. His special fields of interest include VLSI Design, process and device modeling. His name is listed in the science category of Marques Who’s Who USA. He received outstanding achieving ward by the Energy Society, India. He is member of IEEE, ISTE and ISNT.