A High Speed Rail To Rail Micropower Comparator

Prakash Singh Thakur, Praveen Vyas, Mahendra Sakre, Yogesh Dolekar, Kapil Rathi and Dushyant Mehra

***Abstract*- This paper describes precision techniques for the design of comparators used in high performance analog-to-digital converters employing parallel conversion stages. The circuit operates upto supply voltage of 3 Volt and expected to have a typical response time of 52 µSec. and Offset Voltage of about 2.6 mV with a total consumption of 12nA. In CMOS Comparator Offset cancellation is used both a single stage preamplifier and a subsequent latch to achieve an offset of less than 3 mV. The limitation imposed by low supply voltage is presented. The way of Overcoming these limitations based on an accurate sizing of transistor for operation in the weak and moderate inversion regions are studied.**

Keywords: **ADC, CMOS op-amp, IOS, OOS**

I.INTRODUCTION

In high-speed analog-to-digital converters, comparator design has a crucial influence on the overall performance that can be achieved. Converter architectures that incorporate a large number of comparators in parallel to obtain a high throughput rate impose stringent constraints on the delay, resolution, power dissipation, input voltage range, input impedance, and area of those circuits. Moreover, the relatively large device mismatch and limited voltage range that accompany the integration of comparator circuits in low-voltage scaled VLSI technologies severely compromise the precision that can be obtained. This paper introduces design techniques for use in parallel A/D converters that are implemented CMOS VLSI technologies. The suggested methods are intended to provide improved resolution and speed while maintaining low power dissipation, a small input capacitance, and low complexity. The techniques are presented within the context of practical design for a CMOS comparator. In the CMOS comparator, offset cancellation is used in both the preamplifier and the subsequent latch to achieve minimum offset.

II. TECHNIQUES TO MINIMIZE THE OFFSET

A. Circuit Topologies:

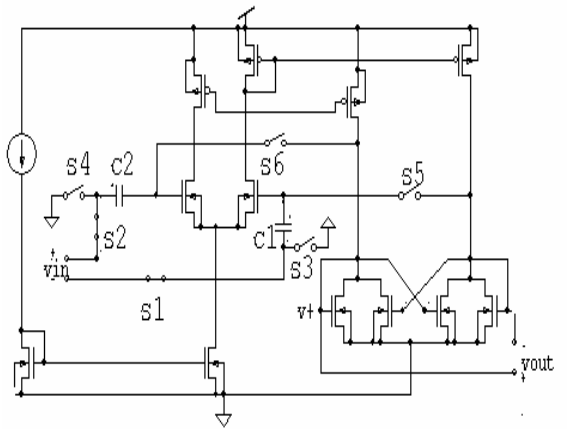
The analog sampling capability inherent in CMOS technologies provides a means whereby offsets can be periodically sensed, stored, and then subtracted from the input of the various offset cancellation methods, two of the most common approaches, based on input offset storage (IOS) and output offset storage (OOS), are considered here in. Fig1 (a) & 1(b). Illustrates these two approaches as applied to a fully differential comparator. These topologies comprise a preamplifier, offset storage capacitors, and a latch. With IOS, the cancellation is performed by closing a unity-gain loop a round the preamplifier and storing the offset on the input coupling capacitors. With OOS, the offset cancelled by shorting the preamplifier inputs and storing amplified offset on the output coupling capacitors. A comparison of these approaches reveals their respective merits and drawbacks. In the comparator with IOS, the residual input-referred offset is:

$$V_{OS} = \frac{V_{OSL}}{1+A_0} + \frac{\Delta Q}{C} + \frac{V_{OSL}}{A_0} \quad \ldots\ldots\ldots\ldots eq.(1)$$ Where

Vosl and Ao are the input offset and gain of the preamplifier, respectively, ΔQ is the mismatch in charge injection from switches S5 and S6 onto capacitors C1 and C2, and Vosl is the latch offset. In the comparator employing OOS, the residual offset is

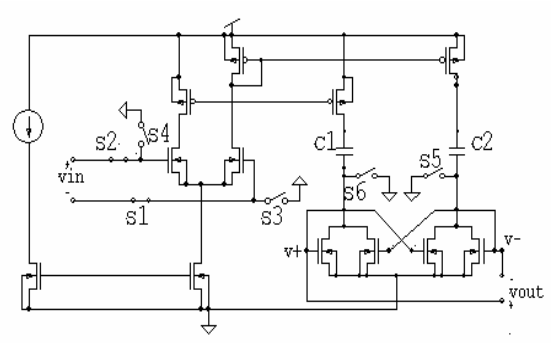
$$V_{OS} = \frac{\Delta Q}{A_0 C} + \frac{V_{OSL}}{A_0} \quad \ldots\ldots\ldots\ldots eq.(2)$$

Eq. (1) & eq. (2) show that, for similar preamplifiers, the residual offset obtainable using OOS can be smaller than that for IOS. In fact, unless sufficient statistical data for Vosl, ΔQ and Vosl are available, IOS requires the use of quite large values for Ao and C to guarantee a low Vos.



1 (a) Input offset storage

Authors are M.Tech. Students of Department of Electronics and Instrumentation SGSITS, Indore (M.P.), India.



1 (b) Output offset storage
Fig1. Comparator offset cancellation technique.

During offset cancellation, the input capacitance of the IOS circuit is equal to the offset storage capacitor, while in the comparison mode it is approximately the sum of the input capacitance of the preamplifier and the parasitic capacitances of the offset storage capacitor. These parasitic capacitances are typically as large as 0.1 to 0.2pF for input storage capacitors in the range of 0.5 to 1pF, whereas the preamplifier input capacitance can be maintained below 30 fF. For this reason OOS is generally preferable in flash stages, where many comparators are connected in parallel. The preamplifier of the OOS topology must be designed for allow gain so that it does not saturate at its output. While IOS is accomplished by means of a closed feed-back loop, which forces the preamplifier into its active region, OOS normally an open-loop operation that requires tight control of the amplifier gain. In CMOS comparator designs, the preamplifier is typically followed by a standard dynamic CMOS latch. This latch has a potentially large input offset and therefore requires the use of a high-gain preamplifier in order to achieve a low offset.

B. Design Constraints in a Dynamic CMOS Latch:

In order to synchronize the operation of a comparator with other parts of a system, as well as provide the gain needed to generate logic levels at the output, a regenerative amplifier is normally used as the final comparator stage. Fig.(2) shows a dynamic CMOS latch similar to that used in to amplify small differences to CMOS levels. In this circuit, when θ is low, M5 is off, S1 and S2 are on, and the latch senses the inputs Vin1 and Vin2.When θ goes high, S1 and S2 turn off to isolate nodes X and Y from input
terminals and M5 turns on to initiate regeneration. In order to simplify calculations and estimate a lower bound for the offset of the latch only the mismatches between M 1and M2 and between S1 and S2 are considered here. In practice, other errors such as mismatches between M3 and M4 further increase the offset. Considering only the M 1, M2 and S1, S2 mismatches, the input offset of the latch can be expressed as:

$$V_{OSM}=\Delta V_{TH}+\frac{1}{2}\left(\frac{\Delta W}{W}-\frac{\Delta L}{L}\right)\left(V_{GS}-V_{TH}\right)+\frac{\Delta Q}{C_D}\qquad eq(3)$$

Where ΔV_{TH} and V_{TH} are the standard deviation and mean of the threshold voltage, ΔW /W and ΔL /L are relative dimension mismatches, $V_{GS}-V_{TH}$ represents the initial gate-source overdrive, ΔQ is the

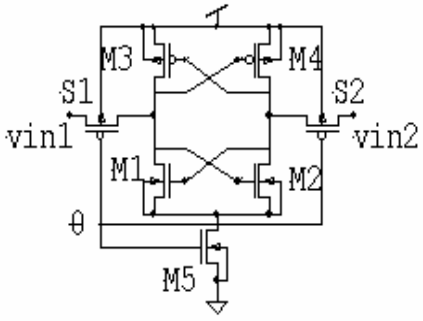


Fig.2: Dynamic CMOS Latch

charge injection mismatch between S1and S2, and C_D is the total capacitance at X or Y. For optimistic values of ΔV_{TH} = 5 mV, ΔW /W = ΔL /L = 0.05, $V_{GS}-V_{TH}$ = 1V, ΔQ = 0.5 fC, and C_D = 100 fF, the latch offset voltage is approximately 28 mV, with its major component arising from the second term in this term can be reduced by increasing W and L and/or decreasing $V_{GS}-V_{TH}$,i.e., decreasing the initial drain current of M 1and M2. However, these remedies can degrade the speed of the latch by increasing the regeneration time constant τ_R. Since

$$\tau_R=\frac{C_D}{g_m}\qquad eq.(4)$$

Where g_m the initial Tran conductance of M 1and M2 is the delay–offset product of this latch assumes the following form:

$$\tau_R V_{OSM}=\Delta V_{TH}\frac{C_D}{g_m}+\frac{1}{2}\left(\frac{\Delta W}{W}-\frac{\Delta L}{L}\right)\left(V_{GS}-V_{TH}\right)\frac{C_D}{g_m}+\frac{\Delta Q}{g_m}\qquad eq(5)$$

This relationship reduces to a simpler form if C_D is assumed to only include the gate–source capacitance of M1or M2, i.e., if C_D = (2/3) WL C_{OX} .Then, substituting for C_D and g_m gives:

$$\tau_R V_{OSM}=\sqrt{\frac{WLC_{OX}}{6\mu_n I_D}}L^{3/2}\Delta V_{TH}+\frac{1}{3}\left(\frac{\Delta W}{W}-\frac{\Delta L}{L}\right)\frac{L_2}{\mu_n}+\frac{\Delta Q}{g_m}\qquad eq(6)$$

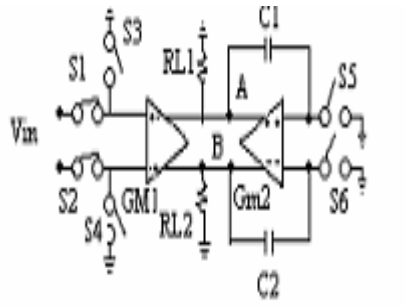
Where I_D is the initial drain current of M 1and M2.Note from above eq.(6) that although increasing L decreases ΔL /L, its overall impact is to increase all of the three terms, thus raising the delay–offset product. In creasing diminishes the last two terms but slowly raises the first term, since the second term contributes most, a W of 5 to10 times minimum size should be used. From above eq (6).it also follows that increasing I_D only slightly improves the tradeoff.

III. SELF-CALIBRATING CMOS COMPARATOR

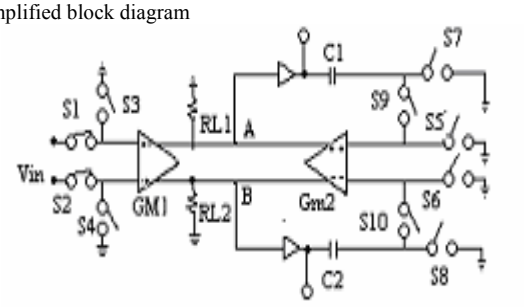
CMOS technology in system design has supported the incorporation of such components in many CMOS processes. To improve the performance obtainable in a fully CMOS comparator, offset cancellation can be applied to both the preamplifier and the latch. The CMOS comparator described in this section employs a topology that achieves complete offset cancellation for both its preamplifier and latch, when implemented in a 0.5μ technology.

A. Architecture:

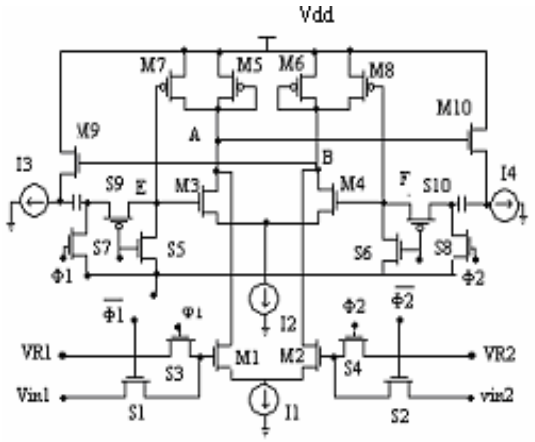
Fig shows a simplified block diagram of the CMOS comparator. It consists of two Tran conductance amplifiers, Gm1 and Gm2, sharing the same output nodes, load resistors R_{L1} and R_{L2}, and capacitors C 1 and C2 in a positive feedback loop around Gm2. In the offset-cancellation mode, the inputs of Gm1 and Gm2 are grounded and their offsets are amplified and stored on C 1 and C2. In the comparison mode, the inputs are released from ground and the input voltage is sensed. This voltage is amplified by Gm1 to establish an imbalance at the output nodes A and B, and hence at the inputs of Gm2, initiating regeneration around Gm2.The calibration of this comparator can be viewed as output offset storage applied to both Gm1 and Gm2, resulting in complete cancellation of their offsets. This topology utilizes the offset-cancelled amplifier Gm2 for regeneration, whereas a conventional OOS configuration incorporates an explicit latch that can suffer from large input offsets. Thus, neglecting second-order effects such as mismatch in charge injection from S5 and S6, the proposed topology achieves zero residual offset while retaining the
advantages of OOS owing to several complications, the block diagram of Fig.3 (a) is not practical.



(a) Simplified block diagram



(b) Modified block diagram



(c) Circuit diagram

Fig.3: CMOS Comparator

First, the feedback capacitors and their parasitic load the output nodes, reducing the speed. Second, because of the finite on-resistance of S5 and S6, the positive feedback loop around Gm2 is not completely broken in calibration mode, making the circuit prone to oscillation. More importantly, when S5 and S6 turn off to end the calibration, any mismatch in their charge injection can trigger a false regeneration around Gm2. Since the feedback is designed for a fast response, this regeneration may not be overridden by small voltages at the input, hence causing a large overall input-referred offset for the comparator. Fig.3 (b). Illustrates a modified comparator configuration that circumvents these problems. In this circuit, buffers B 1 and B2 isolate nodes A and B from the feedback capacitors, while switches S7–S10 disable the feedback loop.

B. Circuit Details :

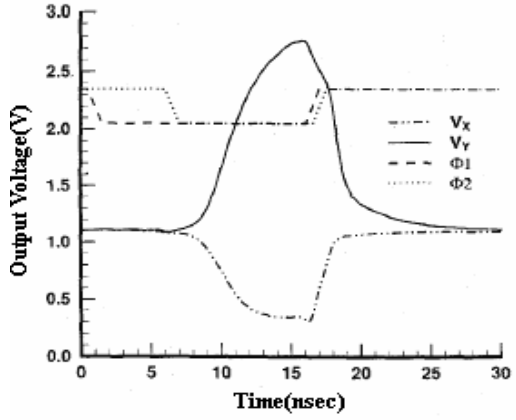
In Fig.3.(c) this circuit, differential pairs M1,M2 and M3, M4 constitute amplifiers Gm1 and Gm2,re-spectively, with source followers M9 and M 10 serving as the buffers B 1 and B2. Transistors M7 and M 8 operates active loads, while M 5 and M6 set the output common-mode voltage and control the gain .The additional currents supplied by M7 and M8 both decrease the voltage drop across M5 and M6 and increase the available gain, two important advantages when the circuit must operate from a single 3-V supply. Moreover, by boosting the currents that charge and discharge nodes A and B, the push–pull operation of M3 with M7 and M4 with M8 improves the large-signal response in two ways: it increases the output voltage swing and enhances the speed. When node E goes high and node F goes low, the current in M7 is reduced, thus allowing M3 to more rapidly discharge node A to a lower voltage, while the current in M 8 is increased, thereby pulling node B more quickly to a higher voltage. Since the comparator of Fig.3(c). includes calibration of both the preamplifier and the latch, its residual offset is due primarily to mismatches among switches S5-S10. This difference results in charge injection mismatch when the two switches turn off and
Charge absorption mismatch when they turn on. In the comparator circuit, both types charge
injection mismatch from of mismatch exist: charge injection mismatch from S5-S8 when they turn off to end

the calibration, and charge absorption mismatch from S9–S10 when they turn on to establish a positive feedback loop around Gm2.Because S5 and S6 discharge their respective nodes to the same potential, their charge injection mismatch can be cancelled by an auxiliary switch placed between nodes E and F that turns off a few nanoseconds after S5 and S6,there by equalizing the voltages at E and F. With the same principle applied to S7 and S8, the charge absorption mismatch between S9 and S10 becomes the only significant contribution to the offset. This offset manifests itself when S9 and S10 turn on, absorb in charge from C 1 and C2 into their channels. The charge absorption mismatch creates an offset voltage between the gates of M3and M4 that is multiplied by the gain of the M3 and M4 pair when it appears at nodes A and B and C is divided by the gain of the M 1 and M2 pair when referred to the main input. The resulting input-referred Offset is:

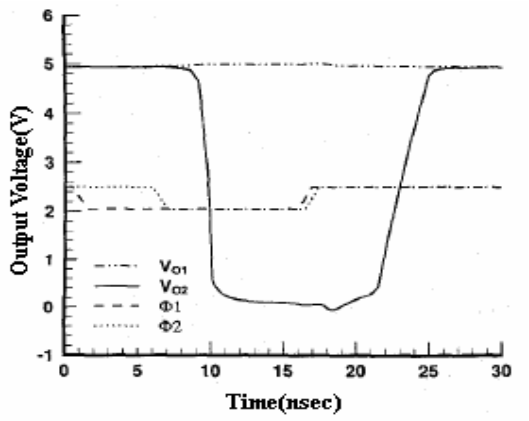
$$V_{OS} = \frac{\Delta Q}{C}\left(\frac{g_{m34} + g_{m78}}{g_{12}}\right)$$

When they are on, C=C1 = C2, and g_{m34}, g_{m78}, and g_{12} are the Tran conductance values of differential pairs M3-M4, M7-M8, and M 1-M2, respectively. This equation indicates that, for a given ΔQ, V_{OS} can be reduced by: increasing C, which increases the recovery and regeneration delays, as well as the area; decreasing $g_{m34}+g_{m78}$,which is accomplished by decreasing I2 and not only degrades the regeneration speed but also lowers the output swing; and increasing g_{12}.As a compromise among these trade-offs, C = 0.5 pF and g_{12} = 2 ($g_{m34}+g_{m78}$) were used in this design. Equation indicates that, in contrast to OOS and IOS configurations, the circuit in Fig. 3.(c) imposes no constraint between the preamplifier voltage gain and the residual offset, thus allowing a better optimization of the load devices for speed and input range.

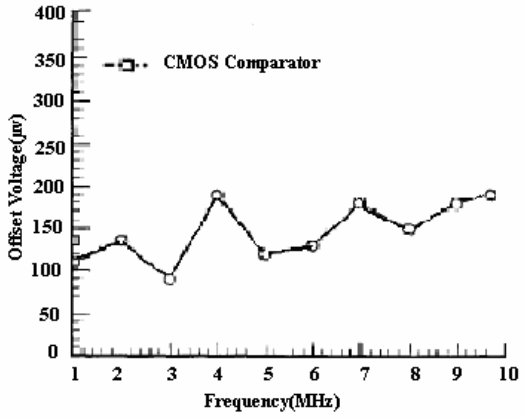
IV. Simulated output results waveform.



(a).Comparator



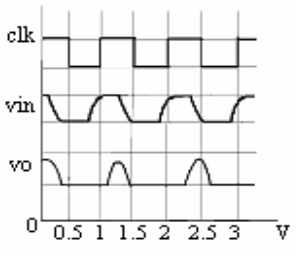
(b)Output Amplifier



(c) Offset of Comparator as a function of frequency

Fig 4. Output waveform

V. Overdrive test recovery of CMOS Comparator:



(a) V_{in1} - V_{in2} = +1mV

(b) V_{in1} - V_{in2} = -1mV

Fig5: CMOS Comparator over drive

VI. PERFORMANCE OF CMOS COMPARATORS

Specifications	Ratings
Input Offset	2.6mV
Comparison Rate	10MHz
Power consumption	12nA
Input Range	2V
Power Supply	3V
Technology	0.5µ
Response Time	52 µS

VII. CONCLUSION

The design of fast precision comparators requires careful trade-offs among parameters such as speed, resolution, power dissipation, and input capacitance. The speed of a comparator is often limited by its pre–amplifier overdrive recovery, while the resolution is constrained by the input offset of its latch. Thus, if the latch offset is reduced in are liable way, the preamplifier can be designed for lower gain and hence faster recovery. The availability CMOS devices on the same substrate can be exploited to design high performance compact analog circuits. A CMOS comparator utilizing a new offset cancellation technique has also been introduced. To achieve a small residual offset, this comparator combines a preamplifier and a regenerative latch, both with offset cancellation. This topology significantly relaxes the preamplifier gain requirements, allowing high speed and low power dissipation. The comparator maintains an offset of less than 3mV with total power consumption of 12 nA.

VII. REFERENCES

[1] Behzad Razavi, Member, IEEE, and Bruce A. Wooley, Fellow, IEEE "Design Techniques for High-Speed, High-Resolution Comparators" IEEE JOURNAL OF SOLID-STATE CIRCUITS. VOL. 27, NO. 12, DECEMBER 1992.

[2] R. Poujoiser al., "Low-level MOS transistor amplifier using storage techniques," in ISSCC Dig. Tech. Papers, Feb. 1973, pp. 152-153.

[3] Benjamin J. McCARROLL, MEMBER, IEEE, CHARLES G. SODINI, MEMBER, IEEE, AND HAE-SEUNG LEE, MEMBER, IEEE," A High-Speed CMOS Comparator for Use in an ADC"

[4] Razavi, Behzad. Design of Analog CMOS Integrated Circuits. McGraw-Hill, pp. 416-423, 2000. Nakamura, Katsu, et al. Digest of Technical Papers.

[5] CMOS Analog Circuit Design by Phillip E. Allen and Douglas R. Holberg (Hardcover - Jun 1995). from CDN$ 135.64. 2. CMOS Analog Circuit Design.

[6] Ramı´rez-Angulo, J., et al.: 'The flipped voltage follower: a useful cell for low-voltage low-power circuit design'. Proc. ISCAS 2002, Scottsdale, AZ, USA, pp. II 615–618

[7] M. Eskiyerli and A. J. Payne, "Square root domain filter design and performance, *"Anal. Int. Signal Process.* vol. 22, pp. 231–243, Mar. 2000.

[8] R. G. Carvajal, A. Torralba, J. Ramírez-Angulo, J. Tombs, and F. Muñoz,"Low voltage Class-AB output stages for CMOS op-amps," in *Proc. of 28th Eur. Solid-State Circuits Conf., ESSCIRC*, Sep. 2002.

[9] J. Ramírez-Angulo, S. Thoutam, A. López-Martín, and R. G. Carvajal,"Low-voltage CMOS analog four-quadrant multiplier based on flipped voltage followers," *Electron. Lett.*, vol. 39, no. 25, pp. 1771–1772, Dec. 2003.

[10] E. Sánchez-Sinencio and A. G. Andreou, Eds., *Low-Voltage/Low-Power Integrated Circuits and Systems: Low-Voltage Mixed-Signal Circuits*. New York: IEEE Press, 1999.

IX. BIOGRAPHY

Prakash Singh Thakur received the B.Eng. degree from Jawaharlal Institute of Technology Borawan, R.G.P.V. University, Bhopal, India, in 2005, and pursuing the M-Tech degree in Microelectronics and VLSI Design from S.G.S.I.T.S. Indore, R.G.P.V. University, Bhopal. His research interests include the design of low voltage, low power, high speed analog design ICs.
E-Mail : psthakur03@gmail.com

Mahendra Sakare received the B.Eng. degree from Jawaharlal Institute of Technology Borawan ,R.G.P.V. University, Bhopal, India, in 2005, and pursuing the M-Tech degree in Microelectronics and VLSI Design from S.G.S.I.T.S. Indore, R.G.P.V. University, Bhopal. His research interests include the design of low noise, low power, fast settling, analog designs ICs.
E-Mail : mahendrasakre@gmail.com

Dushyant Mehra received the B.Engg. Degree from Samrat Ashok Technological Institute Vidisha (M.P), R.G.P.V University, Bhopal, India, in 2004, and pursuing the M-Tech degree in Microelectronics and VLSI Design from S.G.S.I.T.S. Indore, R.G.P.V. University, Bhopal and Member of society of Engineers His research interests include the design of low noise, low power, memories, analog designs ICs.
E-Mail : dushyant_vlsi@yahoo.co.in

Praveen Vyas received the B.Eng degree from M.I.T., Mandsaur (M.P.), R.G.P.V. University, Bhopal, India in 2004 and pursuing M.Tech Degree in Microelectronics and VLSI Design from S.G..I.T.S. Indore, R.G.P.V. University, Bhopal. His Research interest includes the DFTs, Digital and Analog ICs Design.
E-Mail : Praveen_ratlam@yahoo.com

Yogesh Dolekar received the B.Eng. degree from Govt. En.gg. College, Sagar (M.P.), R.G.P.V. University, Bhopal, India, in 2005, and pursuing the M-Tech degree in Microelectronics and VLSI Design from S.G.S.I.T.S. Indore, R.G.P.V. University, Bhopal. His research interests include the design of high bandwidth, low power analog design ICs.
E-Mail : yogesh_dolekar17@rediffmail.com

Kapil Rathi received the B.Eng. degree from Jawaharlal Institute of Technology Borawan, R.G.P.V. University, Bhopal, India, in 2005, and pursuing the M-Tech degree in Microelectronics and VLSI Design from S.G.S.I.T.S. Indore, R.G.P.V. University, and Bhopal. His research interests include the design and verification of low power memories, analog designs ICs
E-Mail : kapil_rathi84@rediffmail.com