Electrical Properties of SOI n-MOSFET at Various Technological Nodes

Rahul Karma, S. S. Rathod and D. R. Mehta

Abstract—**The current interest is focused mainly on the low-voltage/low power digital CMOS applications requiring deep submicron devices. For deep submicron devices Silicon on Insulator (SOI) MOSFETS are superior to their counterparts using bulk CMOS. There is a concern about the suitability of SOI for various electrical parameters especially in the submicron domain. This paper compares the performance of SOI at different technological nodes.**

The focus of our paper is on leakage current, threshold voltage and subthreshold conduction of SOI structures in the submicrometer region. We have constructed soi n-MOSFET using Silvaco-Athena and carried out simulations for leakage current, threshold voltage and subthreshold conduction at 1micron, 90nm and 65nm of technological nodes. Silvaco-Athena structure and simulation results using Atlas are presented, that shows soi technology is still superior in the submicron region. Kink effect analysis is also carried out.

***Index Terms*-- MOSFET, SILVACO-ATHENA, ATLAS, SOI, Subthreshold Conduction, Submicron Technology.**

I. INTRODUCTION

SOI (Silicon-on-Insulator) CMOS technology is becoming another mainstream technology for VLSI. Owing to its inherited characteristics, SOI CMOS technology is especially capable of providing deep-submicron VLSI devices for next-generation high-speed, low-power, system applications using a low-power supply voltage. Thanks to progresses in processing technology, SOI CMOS technology has been used to implement multi-giga-bit DRAM, 1 GHz microprocessors, and other high-speed low-power computer-related VLSI circuits. Owing to much smaller parasitic capacitances, SOI CMOS devices have also been used to integrate high-speed low-power VLSI circuits.

Recently, the demands on low-voltage VLSI circuit designs using deep-submicron SOI CMOS technology have grown dramatically. However, nowadays the development of the supporting environment for meeting the demands on the growth of the SOI CMOS IC designs for VLSI system applications is not paced accordingly. The microelectronics industry is interested in becoming familiar with the SOI CMOS device behaviors and wants to know the performance of SOI in deep submicron region. Multiplicity of unexpected parasitic elements can be formed by the structure. The paper provides brief overview of SOI technology, section II deals with the various electrical parameters under consideration, section III presents the simulation results and discussion.

The cross section of SOI compared to bulk is as shown in fig 1. SOI structures do not vary much from normal bulk CMOS. The major difference is the insertion of the insulation layer beneath the devices. Suppression of bottom junctions lowers parasitic capacitance and makes faster switching and/or lower power dissipation. The full isolation in SOI provide no latch-up, denser layout, lower interferences between the analog and digital parts, lower losses in the passive components at high frequency, lower leakage current, enabling operation at higher temperature (250°C), thin active area and lower sensitivity to radiations [1].

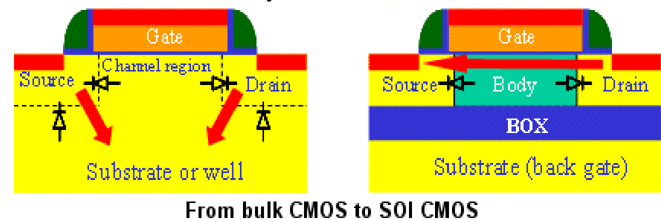

Fig. 1. Migration from Bulk to SOI Structure

II. ELECTRICAL PROPERTIES OF THE SOI MOSFET

Behaviors of SOI CMOS devices are quite different from those of the bulk ones. Understanding the unique behavior of the SOI CMOS devices is important for designing SOI CMOS VLSI circuits.

A. *Threshold Voltage and Leakage Current*

Process variability alters the ratio of forward and reverse diode leakages, which will establish new balanced voltages. Shorter channels will also produce more impact ionization, resulting in more history effect. Conducting Hot Electron generation also simultaneously presents as degradation in device current. This degradation's dependence on channel length, and hence the electron-hole pair generation for a typical production CMOS technology. Shorter channels also produce bodies with less total volume. Smaller bodies contain

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less charge, and the decreased volume reduces the time necessary to achieve large excursions in body potential. Voltage of the supply affects junction leakage, and will affect the body potential. Of importance is not only the magnitude of forward and reverse leakage currents, but changes in the ratio of forward bias current to reverse bias current. Temperature strongly affects junction leakage and device threshold voltage, as well. Lower threshold voltage at higher temperatures increases the portion of the electron energy distribution capable of ionizing silicon lattice points. This again affects the potential where the current into the body is balanced with the current out of the body. Temperature also affects the leakages of the junctions themselves, directly affecting body charge content [5, 6].

The most prominent electrical property of the PD-SOI device is the History Effect [5, 6]. I-V characteristics of the MOSFET built in PD-SOI are no longer constant, but dependent on the amount of charge contained in the body of the device at any given time. The charge content of the body and the distribution of that charge caused by gate, source, and drain potentials determine the behavior of the device. Charge in the body is directly related to the potential of the body.

The dependence of MOSFET threshold voltage on substrate bias is well known. Conceptually, body bias's effect on threshold voltage may be explained by how strongly this potential reverse-bias the junctions, which must be overcome by gate drive. The magnitude of charge contained in the body is dependent on a number of factors which include: *Previous state of transistor, Schematic position of transistor (possible source, drain voltage ranges), Slew rate of input, and load capacitance, Channel length and processing corner, Operating supply voltage, Junction temperature, Operating frequency and specific switch facto.*[5, 6]

B. Subthreshold Analysis

The Subthreshold behaviour of an SOI MOS device depends on the thickness of the silicon thin-film, the doping density of the silicon thin-film, and the channel length. When the silicon thin-film is thick, partially depleted, the subthreshold slope of the SOI n-MOSFET device is similar to that of the bulk devices. When the silicon thin-film is thin, fully depleted, its subthreshold slope is much better with its value close to the ideal case due to the buried oxide isolation between the channel and the grounded substrate. For a partially depleted device, a higher silicon thin film doping density leads to a worse inverse subthreshold slope silima to the bulk device [2, 3].

A hump in the subthreshold characteristics can be be ssen in mesa isolated SOI n-MOSFETs. The hump is caused by the 2D effect, which results in a smaller threshold voltage for the sidewall channel as compared to the center channel [2, 3].

C. Kink Effect

PD-SOI MOSFET transitions from accumulation into inversion and saturation, it moves through an interval of gate drive in the *conducting mode* where impact ionization peaks, generally at VDD/2. The injection of positive charge into the body has a noticeable effect on the dynamic behavior of the device. Because a large sudden increase of positive charge will reduce threshold voltage, a *kink,* or increase in I_{DS} may be observed when the gate voltage reaches approximately VDD/2. This change in slope, observed at normal operating voltages, is often referred to as the "First Kink." [4]

A second kink, not nearly as noticeable as the first kink occurs after the first kink. As the device current increases, the body-to-source diodes can eventually forward-bias, enabling the flow of bipolar current in the structure. This bipolar device, in parallel with the intended MOSFET, tends to augment the MOSFET. For most practical applications, this second kink is usually overlooked.

A third kink, of sorts, may be observed when the device is operated at elevated voltages, as practiced during reliability stress testing. As the supply voltage increases, the kink just described first appears at lower and lower gate voltages; at a sufficiently high VDD, impact ionization in the device's *non-conducting mode,* with the gate voltage at GND, causes positive charge to accumulate in the NFET body, depressing threshold voltage before the gate is even turned on. The second kink is a concern when stressing parts at elevated voltage and temperature, when functionality is still required. The naturally lower threshold voltages caused by elevated stress temperatures exaggerates this impact ionization, further threatening circuit functionality.

Thus kink occurs because of impact ionization which charges the body of the device and raises body bias. It follows, then, that the more time the gate potential spends in the device region of operation which maximizes impact ionization, the more noticeable the kink will be i.e. the "amount" of kink would be expected to vary with gate switching frequency [4].

III. RESULTS AND DISCUSSION

The SOI n-MOSFET is constructed using Silvaco Athena at various other technologies e.g. 65nm, 90nm, 1um and 3µm[7]. The developed device consists of thin gate oxide. The device structure of SOI n-MOSFET at 1µm is as shown in fig.2.

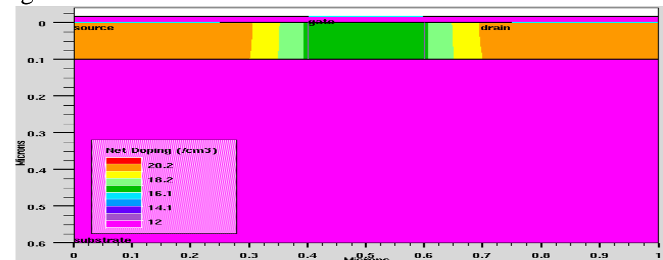

Fig. 2. SOI Device Structure of MOSFET at 1micron

The plots for the leakage current of SOI n-MOSFET at 1µm, 90nm and 65nm is as shown in fig. 3, fig. 4 and fig 5. The leakage current of corresponding default CMOS model from Silvaco-Athena [7] is found to be much more than SOI models. When SOI models are compared for different device sizes then leakage current increases as the device size shrinks as indicated by table 1.

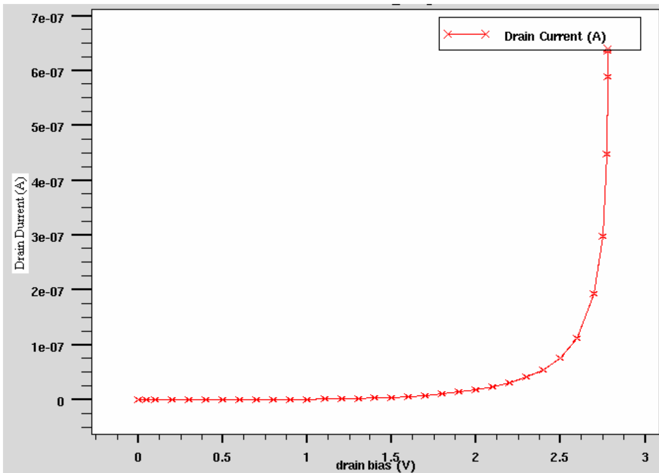

Fig. 3. Leakage Current of SOI MOSFET at 1 micron

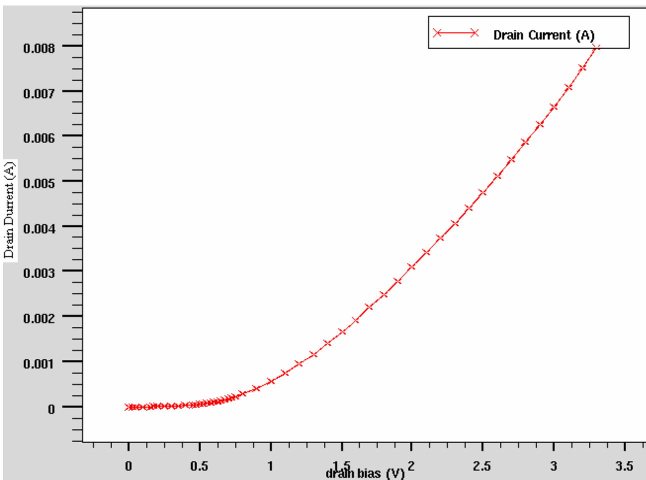

Fig. 4. Leakage Current of SOI MOSFET at 90nm

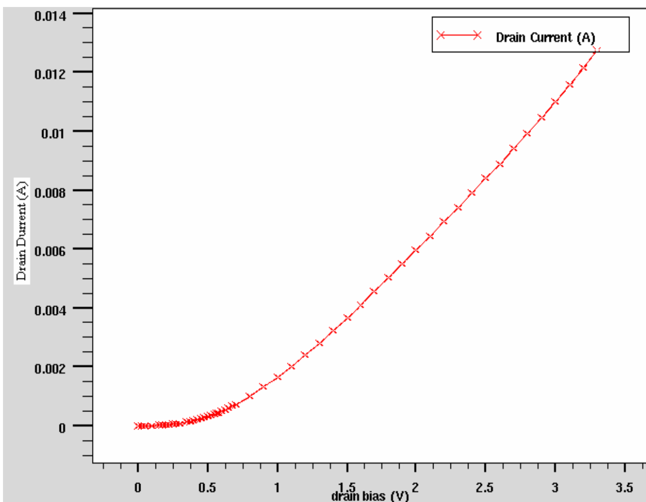

Fig. 5. Leakage Current of SOI MOSFET at 65nm

The plots for the extracted threshold voltage of SOI n-MOSFET at 1µm, 90nm and 65nm is as shown in fig. 6, fig. 7 and fig 8. The threshold voltage of corresponding default CMOS model from Silvaco-Athena [7] is found to be much more than SOI models. When SOI models are compared for different device sizes then threshold decreases as the device size shrinks as indicated by table 1.

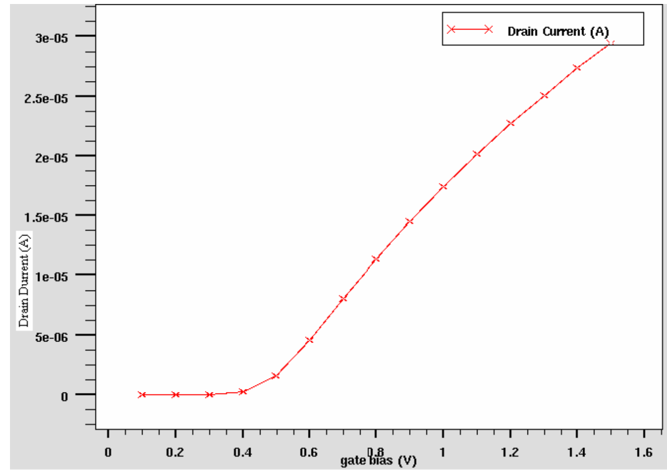

Fig. 6. Threshold Voltage of SOI MOSFET at 1 micron

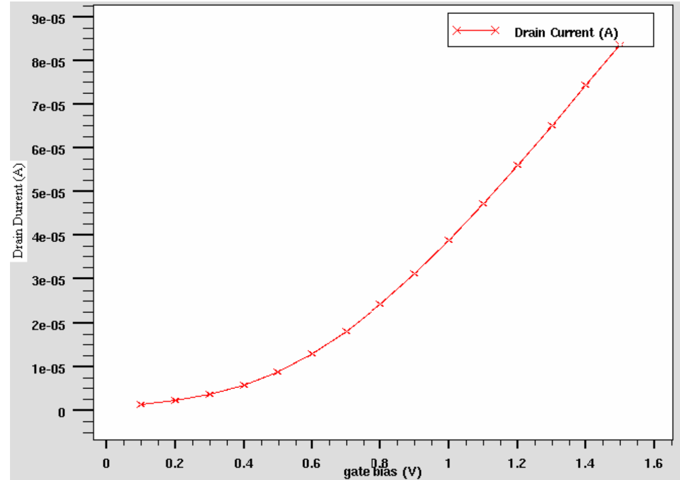

Fig. 7. Threshold Voltage of SOI MOSFET at 90nm

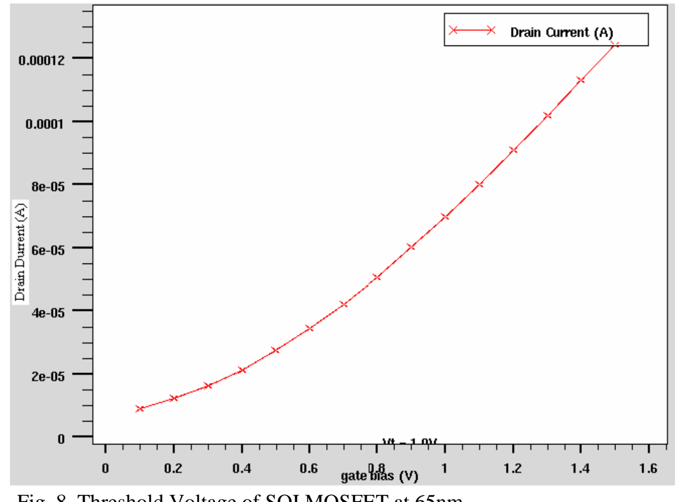

Fig. 8. Threshold Voltage of SOI MOSFET at 65nm

The plots for the subthreshold conduction of SOI n-MOSFET at 1µm, 90nm and 65nm is as shown in fig. 9, fig. 10 and fig 11. The subthreshold current of corresponding default CMOS model from Silvaco-Athena [7] is found to be much more than SOI models. When SOI models are compared for different device sizes then subthreshold current increases as the device size shrinks as indicated by table 1.

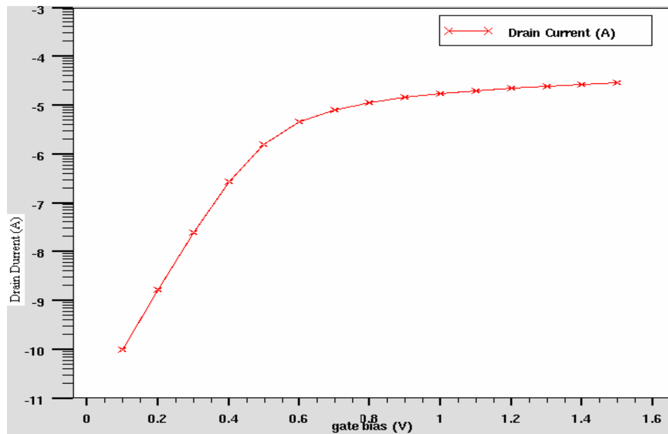

Fig. 9. Subthreshold Conduction of SOI MOSFET at 1 micron

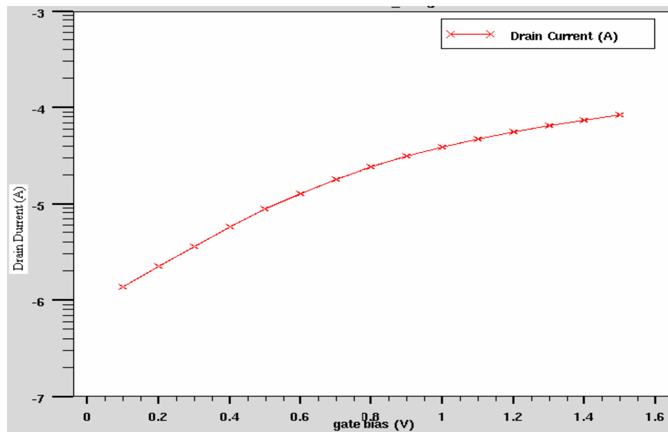

Fig. 10. Subthreshold Conduction of SOI MOSFET at 90nm

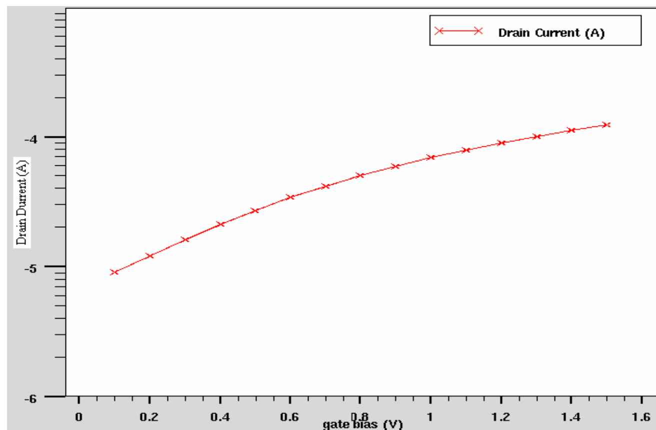

Fig. 11. Subthreshold Conduction of SOI MOSFET at 65nm

The Atlas [8] simulation is also carried out for the kink effect at 3µm and 1µm technology as is as shown in fig 12 and fig. 13. The plot clearly indicates various kink points at different V_{GS} voltages. It also shows that the curve becomes smooth for the lower dimensions of the device.

Table 1 shows the increase in the leakage current, decrease in threshold voltage and increase in subthreshold voltage/decade from the extracted values of 2D device simulation [7, 8] of n-MOSFET using Silvaco-Athena.

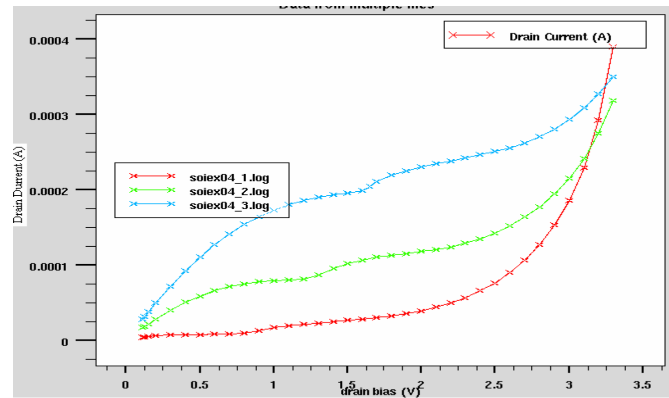

Fig. 12. Kink Effect of SOI MOSFET at 3micon

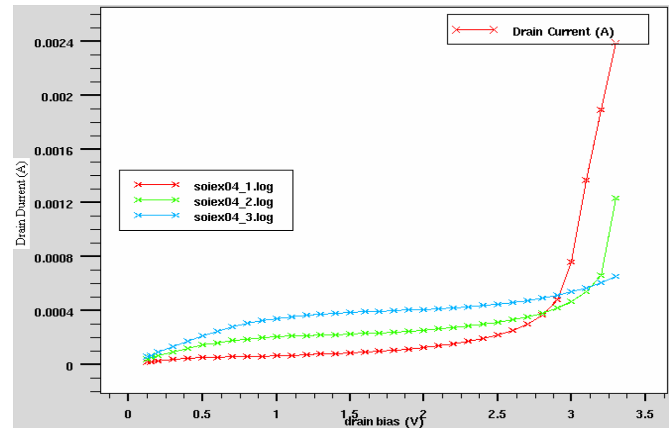

Fig. 13. Kink Effect of SOI MOSFET at 1micron

TABLE I

THE EXTRACTED VALUES OF THE LEAKGE CURRENT, THRESHOLD VOLTAGE AND SUBTHRESHOLD VOLTAGE AT DIFFERENT TECHNOLOGICAL NODES.

Technology	ids_leakage (A)	Vt (V)	Subvt (V/decade)
3micron soi	4.418e-14	1.00227	0.00773
1micron soi	6.42171e-07	0.619941	0.08123
90nmsoi	7.97791e-03	0.56231	0.464582
65nmsoi	12.7806e-03	0.36122	0.77536

IV. Conclusions

The developed SOI n-MOSFET structure using process simulator Silvaco-Athena at 3µm, 1µm, 90nm and 65nm is compared for the various electrical properties. As compared to the bulk device n-MOSFET structure, SOI shows the improved electrical characteristics. But when scaling continues in SOI, the parasitic effects will also appear increasing the leakage current and sub threshold conduction.

V. Acknowledgment

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VII. BIOGRAPHIES

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