CPLD Make a Speech Transfer Process Secure on a Chip

Rohita Jagdale, Namrata Mahender and Manish Patil

Abstract— **This paper presents a design of speech security system in system programmable CPLDs. A privacy arrangement for a communication system scrambles the analog input signals by scrambling technique & encrypted data is finally transmitted. At the receiving end the signal is reconstituted or decrypted by using the same approach. The main objective of this technique is to provide security to the individuals with reliable and safe transmission without intermission of the third party.**

Keywords -- **CPLD, Receiver, Security System, Transmitter, VHDL, VLSI**

I. Introduction

INFORMATION security is more and more important nowadays. In this information age, individuals right must be protected from eavesdroppers. This includes their legitimate personal and business transactions. We need some mechanism to ensure the privacy [1], [2], [8] authentication, and integrity in the voice communication. By using an encryption technique, individuals can be reasonably sure and feel confident that no one or third parties eavesdrop the conversation. Moreover each individual can be certain of other party's identity.

The main feature of this system is to make speech transfer process more secure using Xilinx CPLDs [2]. By implementing it in the hardware, the system will become fast and secure.

The general idea of the speech transfer system [1] is shown in Figure 1. At the transmitting station a signal source, which, in the ordinary case, is a microphone? The output of the source is passed through conditioning circuits, which may amplify it and filter it before passing it to an encryption module. An encryption module modulates the signal and transfers it to the receiver.

At the receiving station the incoming signal is passed through the signal conditioning circuit [2], [3]. It is then feed to a demodulator whose output is same as the scrambled output of the transmitting station.

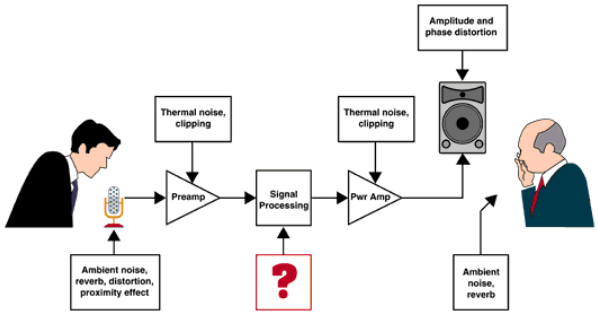

Figure 1. Typical Speech Security System

II. Hardware Module of the System

The Hardware Module of the System is shown in Figure 2. It consists of two major parts, as transmitter and receiver. Both are designed using XC95108 CPLD [3], [4], [5] chips, those are working as central processing unit at transmitter and receiver.

A. Transmitter Module

At the transmitter, signal from the mic is amplified and filtered before passing to analog to digital converter 0809. ADC converts this analog signal into equivalent eight bit digital data. This data is encrypted inside transmitter CPLD [6], [7] using scrambling technique written in VHDL. According to E/D switch position this data is transferred to the receiving stations using I^2C bus protocol technique.

B. Receiver Module

At the receiver, two receiving stations are designed as Receiver 1 and Receiver 2 in a single CPLD [2]. Data reception module is written in VHDL while considering dedicated hardware of I^2C bus protocol compatible with transmitter. According to E/D switch position particular

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receiving station will receives data serially from transmitter. If E/D switch position is 01, Receiver 1 will receives data, if E/D switch position is 10, Receiver 2 will receives data and if E/D switch position is 11, then both receivers will be receiving data. Receiver will de-scramble that data and gets original data back. This data is then passed to DAC 0808 and get original analog signal, filtered and amplified it and transfer it speaker.

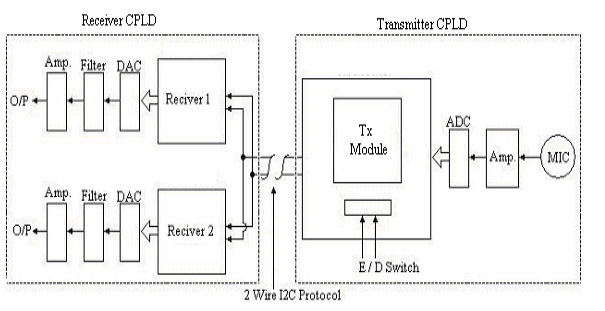

Figure 2. Hardware Module of the System

III. Implementations inside CPLD devices

CPLD implementation of speech transfer system is done with VHDL with the help of Xilinx Web pack ISE 5.1 & Modelsim.

A. RTL View of transmitter

Figure 3 shows RTL view of the transmitter generated in Project Navigator. It consists of 8-bit data input of the CPLD [3], eoc, ale, start, addr (2:0) are the control lines for ADC. i2c_clk & i2c_data are the outputs of the transmitter.

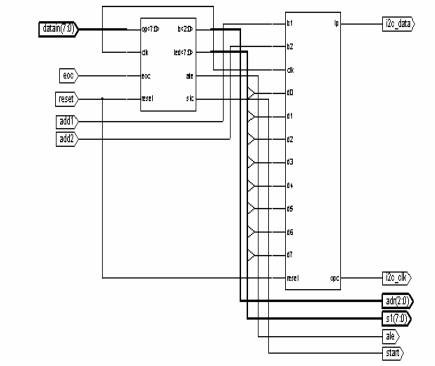

Figure 3. RTL view of the Transmitter

B. RTL View of the Receiver

Figure 4 shows RTL view of the receiver generated in Project Navigator. It consists of sdata & sclk as inputs and dout1 & dout2 are the outputs of the receiver 1 & receiver 2 respectively.

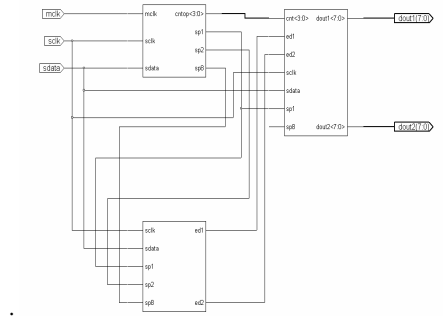

Figure 4. RTL view of the Receiver

IV. Simulation waveforms

The figure 5 shows the simulation waveforms of the transmitter. To check the working of the transmitter provides analog input to ADC from potentiometer or function generator. ADC will convert analog signal into its equivalent digital data. This data is input to CPLD e.g. the data shown in figure is datain as 11110000. CPLD scramble this data and transfer i2c_data signal as 00001111 serially towards receiver.

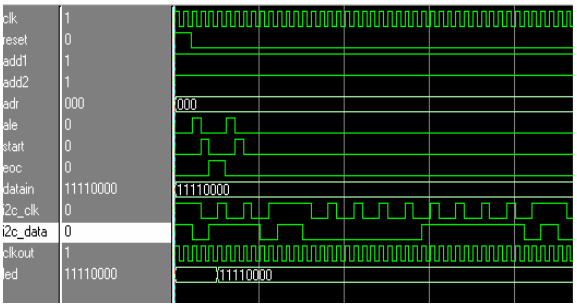

Figure 5. Simulation waveforms of the transmitter

The figure 6 shows the combined waveforms of the transmitter & receiver. Here datain is the input of transmitter, dout1 & dout2 are the outputs of the Receiver 1 and Receiver 2 respectively.

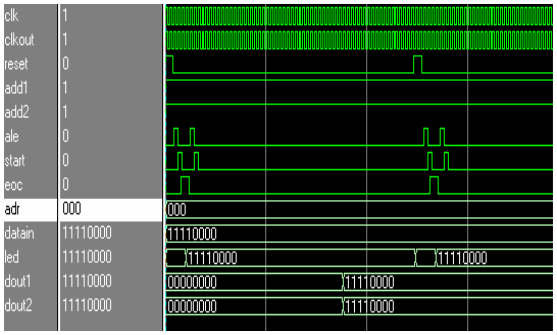

Figure 6. Combined Simulation waveforms of the Transmitter & Receiver

V. CONCLUSION

In this paper we have discussed the implementation of Voice Security System inside the CPLD. The major advantage is the secure and reliable transmission of data without any intrusion; secondly the speed is much higher due to the hardware deployment of the technique as compared to the software implementation.

VI. REFERENCES

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