Design Overview of Low Power Implantable Pacemaker Using MSP 430F1612

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Abstract--Processor is an important computing element in real time embedded system. Implantable pacemaker being a very crucial device for human being, low power design is a challenging phenomenon. In hardware/software codesign methodology, processor consumes most of the battery energy. Generally custom based embedded chip design increases cost and time to market. In this paper Texas Instruments ultra low power MSP 430F1612 processor is used for the implantable pacemaker design. Implantable Pacemaker generates programmable parameters like pacing pulse, pulse width refractory pulse, to stimulate diseased heart. Code developed for these is tested analytically with respect to average current consumption. Out of various functional blocks of pacemaker, ECG sensing is experimented and tested. Experimentation in VVI mode is carried out using MSP430F1612 target board and IAR workbench. Methodology used, seems to be powerful to test and develop low power design strategy to increase battery longevity.

Index Terms--ultra low power, pacemaker, embedded system, Hardware/software codesign, current consumption, low power modes, Electrocardiogram (ECG), pacemaker modes.

I. INTRODUCTION

ELECTRICAL pulses generated by Sinoatrial node (SA) are responsible for the contraction and dilation of heart muscles. These electrical impulses take care of heart muscle synchronization and hence blood pumping. Heart generates an electrochemical impulse that spreads out in the heart which causes cells to contract and relax in timely order. Specialized cells which produce such impulses are known as Pacemaker cells and specialized portion of the heart which creates these impulses is known as Sinoatrial (SA) node. Although, all the heart cells possess the ability to generate electrical impulses or action potentials, SA node is responsible for the whole heart's beat. After contraction of the atria, the impulse proceeds to the AV node. The impulse

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slows at the AV node, which allows time for contraction of the atria. Just below the AV node, the impulse passes quickly through the bundle of His, the right and left bundle branches and the Purkinje fibers and lead to contraction of the ventricles as shown in figure 1. In case of damaged intrinsic conduction system, an artificial device known as pacemaker is implanted within the heart. Cardiac pacemaker is used to treat bradycardia. Device monitors the heart rate and stimulates heart when it beats too slow or does not beat and main goal of cardiac pacing is to artificially stimulate a diseased heart to operate at normal rate. An artificial pacemaker is a device that delivers a synchronized rhythmic electric stimulus to the heart muscle in order to maintain an effective cardiac rhythm for long periods of time. Pacemaker system consists of device and leads. Flexible insulated unipolar/bipolar leads with electrode tip are inserted through vein into the heart. These carry impulses from the pacemaker device to the heart, to stimulate. Similarly information is transferred from heart to the device. Implanted pacemaker is battery operated real time embedded system which must be smaller in size and less in weight. Pacemaker works in three operating modes.

- Free running (fixed or asynchronous): It is insensitive to any rhythm that may develop in paced chamber.
- Inhibited: It senses cardiac activity and does nothing if this is present, but delivers a stimulus after an elapsed time if no further cardiac activity occurs to inhibit operation.
- Triggered- senses activity and delivers a stimulus in a desired way.



Fig. 1. Electrical conduction system of Heart.

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Implantable pacemaker utilizes the energy stored in batteries to stimulate the heart and pacing drains more current from the pulse generator power source. Pulse amplitude, pulse width and pacing rate will affect longevity of the battery. Though modern batteries having high energy density and low self discharge rate like lithium iodine are used in it, energy budget is limited. Hence low power hardware/software codesign methodology is important to increase longevity of the battery and surgery period too i.e. upto 10 to 12 years. In advanced pacemaker, optimized hardware-software codesign is used. Hardware software codesign is used in modern systems for flexibility in operation. Software enhances the capabilities of the pacemaker making it diagnostic tool besides the typical characteristics. Pacemaker has following parameters as shown in figure 4

- Basic pace interval: The basic pace interval is the period of time that pacemaker awaits to apply stimulus to the heart. It is measured in beats/min.
- Escape interval: The escape interval is the period of time that the pacemaker awaits after a spontaneous QRS has been generated. It is measured in ms.
- Ventricular Refractory period (VRP): The VRP is the amount of time that the sense circuit is turned off. This is done to avoid sensing the pacemaker own stimulus, the paced QRS complex, T wave and after potentials. If the sensing circuit is no turn off, then it will generate stimuli to all these events, causing ventricular fibrillation. It is measured in ms.
- Pulse width: It is the amount of time the pulse generator will supply the stimulus to the heart. This parameter is important to capture heart. The pulse width is measured in ms.
- Pulse Amplitude (Volts)
- Sensitivity: It is minimum threshold voltage of an input signal that sets a flag in ultraslow power processor. This parameter is measured in mv.
- Pacing and sensing Electrodes: Unipolar and Bipolar electrodes.
- Modes of operation: North American Society of Pacing and Electrophysiology (NASPE) and British pacing and Electrophysiology (BPEG) as shown in table 1 ,used nomenclatures to classify pacemakers like VVI, VVT, VOO, AAI, AAT and AOO. For example VVI means Pacemaker sense the ventricle and pace the ventricles in inhibited mode.[3,10,11]



Fig.2. Typical Index 186, Left Ventricular Endocardium (ECM) waveform [15]



Fig.3. Typical 12 Surface Lead ECG waveforms [15]



Fig. 4. Pacemaker's programmable timing parameters.

Modern implantable pacemaker uses, VLSI based analog/digital custom design with interfacing peripherals, which increases cost and time to market. Ultra low power microcontrollers along with necessary are available today which will be better choice for power crucial biomedical applications.

II. PACEMAKER SYSTEM OVERVIEW AND DESIGN REQUIREMENTS



Fig.5. Implantable Pacemaker block diagram

Implantable pacemaker needs front end interfacing circuit to capture heart signals, computing element with peripherals and output multiplier/pulse generator to stimulate heart. Electrogram (EGM) and Electrocardiogram (ECG) are the heart signals sensed by intracardiac and surface electrodes as shown in figure 2 & 3 respectively. The front end senses the voltage generated by the pumping action of the heart, which is small signals with many noise components. Sensing is performed using intracardiac / surface unipolar or bipolar electrodes. Cardiac signal is amplified by a low noise preamplifier, gain amplifier and filtered by second order low pass filter to get appropriate ECG/EGM. This signal is applied to the comparator. Comparator circuit is used as a threshold detector, to detect the heart beat event executed by the heart and generates a pulse with every heartbeat. Reference signal generated by inbuilt Digital to Analog converter is applied to the comparator. The resulted pulse from the threshold detector is given to the non retriggerable monostable multivibrator which eliminates chances of triggering multivibrator due to noise and artifacts. Synchronizing pulse is applied to the inbuilt 12-bit Successive approximation type Analog to Digital converter.

System also consists of battery management system for monitoring battery status. Battery power management system monitors the status of the battery and gives indication about the battery condition. Battery voltage is monitored by the internal Supply Voltage Supervisor of the MSP430F1612.SVS can be programmed to to detect low battery voltage. In case of low voltage condition SVS sets a interrupt flag. Conventionally the status of the battery is determined by measuring its output voltage. Output stage called charge pump, consists of voltage multiplier/pulse generator to stimulate heart. A high voltage pulse of 5V or above is delivered to the heart through pacing electrodes. The amplitude and pulse width must be customized for each patient [1].

Implantable Pacemaker is a computer controlled real time embedded system in a single unit with hermetically sealed titanium encapsulation, to pace the abnormal heart. Microcontroller with optimized software is basic component in it. Microcontroller to be chosen must have low power consumption and required memory. It must operate with at least 2V and drains supply current in microamperes order in standby mode. It is better to select ultralow power microcontroller with specific inbuilt peripherals like ADC, DAC, DMA, Supply Voltage Supervisor, Comparator etc.

For implantable pacemaker, selection of battery plays a very crucial role. There are two main chemical batteries for pacemakers, the Mercury –Zinc battery and Lithium Iodine battery. Mercury Zinc batteries contain a porous zinc cathode and an anode composed of a composed mixture of mercuric oxide, graphite and sliver oxide. The electrolyte is largely potassium hydroxide. The open circuit voltage is 1.35 and typical cells provide 1 ampere-hour of charge when discharged at 40 A. The power density is on the order of 500mW-hr/cm3 of cell. In Lithium Iodine cells the anode is lithium and the cathode is iodine. In this battery no gas is liberated. The open circuit voltage of the cell is 2.8 V and has

ratings of 2 amperes-hours. The power density is similar to or slightly higher than that of the mercury zinc cell. Since no gas is liberated the cell can be completely sealed. Lithium Iodine batteries are standard in modern pacemaker [3, 7]. Typical characteristics for a standard lithium iodine cell are given in [8]. Various peripherals customized as shown in figure 5 are integrated in MSP 430F1612 ultra low power microcontroller.

TABLE I BPEG OPERATING MODES

Position	Category	Code
	Chamber(s)	O=None
I	Paced	A=Atrium
		V=Ventricle
		D=Dual(A+V)
П	Chamber(s)	O=None
	Sensed	A=Atrium
		V=Ventricle
		D=Dual(A+V)
Ш	Response to	O=None
	sensing	T=Triggered
		I= Inhibited
		D=Dual(T+I)
IV	Rate	O=None
	Responsive	R=Rate
		Modulation
V	Multirate	O=None
	Pacing	A=Atrium
		V=Ventricle
		D=Dual(A+V)

 TABLE II

 POWER DOWN MODES OF MSP 430 SERIES [13]

Power Down	Description	Current consumption	
Modes		VCC=3V	VCC=2.2V
AM	All clocks are	340 µA	225 μΑ
	active		
	CPU and MCLK		
LMP0	are disabled,	70 µA	65 µA
	AUXCLK and		
	SCLK are active		
	CPU, MCLK,		
	SMCLK, DCO		
LPM2	osc. are disabled	17 µA	11 µA
	.DC generator	-	-
	remains enabled,		
	ACLK is active		
	CPU, MCLK,		
	SMCLK, DCO		
LPM3	osc are disabled.	2 µA	1 µA
	DC generator		-
	disabled, ACLK		
	is active		
LPM4	CPU and all	0.1 µA	0.1 µA
	clocks are		-
	disabled		

III. ADVANCED FEATURES OF MSP 430F1612 ULTRA LOW POWER PROCESSOR

The Texas instruments MSP 430 family of mixed signal microcontroller has Von Neumann, RISC instruction set, 3-stage pipeline and 16 bit data processing architecture. The MSP 430F1612 has inbuilt peripherals such as two 16 bit timers, a high performance 12 bit A/D converter, dual 12 bit D/A converters, one USART, DMA, 48 I/O pins, comparator digitally controlled oscillator (DCO) and SVS etc. The device is a powerful 16 bit RISC CPU with 16 registers. The digitally DCO has a wake up time of 6 µsec. to shift from low power modes to active mode.

It has five low power modes to extend battery life in portable energy crucial biomedical applications. Power down modes as shown in table 2, are among the most important features enabling the microcontroller unit to meet the current budget. Low power modes LMP0 turned off CPU and leave everything else functional. Modes LPM1 and LPM2 add various clocking functions to the list of disabled functions. LPM3 is the most used low power mode leaving only a low frequency clock oscillator running and any peripheral that uses that clock, LPM3 is often called the real time clock mode because it allows a timer to operate for low power 327658 Hz. Clock source consuming less than 1 µAmp and periodically wake the system for activity. Finally LPM4 turns off all clocks on the device thus turning off any peripheral that used clocks automatically. Analog peripherals may still be active but if none are, LPM4 current consumption is only 100 nano amps, including RAM retention. Current drain for the low power modes is given in figure 6.

MSP 430F1612 processor has special features like 1.1 μ A standby current, Low supply range (1.8 to 3.6 V),ultra low power consumption ,five power saving modes, wakeup time from standby to active mode is less than 6 μ sec, 12 bit A/D converter with internal reference ,sample and hold and auto scan feature, SVS ,60KB flash memory and 5KB RAM, comparator [12,13].



Fig.6. MSP 430, typical current consumption.

IV. PACEMAKER DESIGN CONSTRAINTS AND METHODOLOGY

Embedded computer system is hardware/software codesign with dedicated processor. As most of the embedded portable devices are battery operated, low power design methodology plays a crucial role in design. A large number of embedded computing applications are power critical and power constraints form an important part of the design specification. Processor is an important computing element in battery operated real time embedded system and consumes most of the battery energy [6]. Even with advanced battery technology, power budget is limited. Appropriate /optimized software design and analysis became a latest trend in modern embedded systems.

Artificial pacemaker is a battery operated system implanted in the heart through surgery. Current consumption plays an important role to decide battery longevity. To design intelligent pacemaker system microcontroller is a main computing element. Microcontroller consumes most of the battery energy. It should drain current in microamperes and should operate with 2V to 3V battery voltage. Like hardware, software is also responsible for the power consumption. Considering average current consumption, available power down modes, clocking system, pin leakage, internal peripherals such as ADC, DAC, SVS and ultra low power functionalities etc, TI's MSP 430 series microcontroller is selected for pacemaker design. Design methodology includes software/Hardware design, Integration & Verification etc. Pacemaker should sense and stimulate the heart with unipolar or bipolar polarities. It operates using a lithium battery of 3V and works for supply voltages from 2V to 3V. It should offer a wide range of programmability, including basic pace rates, pulse widths, pulse amplitudes, Escape (hysteresis) intervals, sensitivities and polarities. It should operate in various modes such as VVI. VVT. VOO. AAI. AAT and AOO etc. The whole system is intended to have low power consumption and a life of 10 to 12 years when using 2Ah rate.

V. STRATEGY IMPLEMENTATION AND REALIZATION

In this research work, code is developed for the interrupt handlers for pacing pulse, pulse width, refractory pulse. Similarly code is developed for the EGM/ECG sensing. Software simulation gives cycles to execute each instruction and complete program. TI's IAR workbench is used for code simulation and MSP 430F1612 target board as shown in figure 7, is used for ECG sensing implementation. Test ECG signal is taken from Scientech ST 2351 ECG trainer kit, for experimentation. DAC output and ECG sensing results as shown in figure 8, 9&10, are monitored using Tektronix TDS 2024 Digital Storage Oscilloscope. Theoretical current measurement scheme is used to measure processor current while executing instructions.



Fig.7. MSP 430F1612 Target Board



Fig.8. DAC output



Fig.9. Sensing pulses at pin 38, ECG and synchronizing pulse

A. Software Strategy

As mentioned in section II, Basic Pace interval, Ventricular refractory period, pulse width, and ECG interrupt needs timer. There are two timers, Timer A and Timer B in MSP430F1612. Timer B is used to count intervals and generate interrupts accordingly. In this application four interrupts are used initially .i.e Basic Pace interrupt, Pulse width interrupt, Refractory interrupt and ECG interrupt. ECG signal is sensed from the heart and converted into digital signal using internal ADC.ECG interval defines the rate at which ECG is sampled and converted into digital data. To pace the heart in abnormal heart situation ECG interrupt is used. These interrupts are mostly operated by hardware. Timer B interrupts uses TBCCR1, TBCCR2, TBCCR3 and TBCCR4 registers for basic pacing, Pulse width, refractory, and ECG interrupt respectively. Timer counts the programmed parameters and generates interrupts to apply stimulus to the heart. Programmed parameters like Basic pacing rate (74 bpm), Pulse width (1.50 ms) and Refractory period (305ms), activates interrupts. Codes for these interrupt are developed and tested using, IAR workbench and MSP430F1612 target board.

B. Current Measurement and Battery longevity

Instruction level based current analysis technique developed in [3, 5] is implemented to measure the processor current consumption. Instruction level power model is developed for the pacemaker software and used to evaluate it. As power consumption of processor varies from program to program and as there is no tool available today to evaluate the power performance of software, this strategy seems to be powerful. In this strategy, base cost of each instruction is measured using dual slope integrating digital ammeter. The base cost of a given instruction is defined as the average current drawn by the processor during repeated execution of the instruction. To calculate total processor current consumption executing instruction, base cost and cycles are used. MSP 430 series has 27 basic instructions. Base cost of each instruction is measured thereby executing each instruction in loop [2]. Out of various power down modes LMP3 Mode which has 2 µAmp standby current is used in this application. As shown in figure 10, if 1 mAmp activity occurs for 1 msec. through interrupt, average current will be $3 \mu A$ [6]. Same strategy is implemented in this paper to calculate current for each interrupt handler program and to extend the battery life given by equation (2).



Fig.10. Average Current distribution in MSP 430 processor

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Let $P = \{I1, I2, I3$, In $\}$	
I1A1 μAmp, C1 cycles	
I2 A2 µAmp, C2 cycles	
I3 A3 µAmp, C3 cycles	
In An µAmp, Cn cycles	
Where P Program	
I1, I2, I3,In Instructions	
A1, A2, A3,An base cost	
C1, C2, C3, Cn Cycles to execute Instructions.	
Average current (Iav).	
= A1*C1+A2*C2+A3*C3++An*Cn (1)	
C1+C2+C3++Cn	
Battery life = Battery rating in Amp.Hour (2)	
Current	
For Example: Each Interrupt handler consists of set of	f
instructions as given in table III, IV, V,VI.	
Average Current according to Equation (1)	

0	0			
For Basic pacing	; interrupt	handler	=	339.723 µA
For Pulse width	interrupt h	andler	=	332.8 µA
For Refractory p	eriod inter	rupt handler	=	335.757 µA
For ECG interru	pt handler		=	335.162 µA

TABLE III BASIC PACING INTERRUPT INSTRUCTION SET

	Base	Number
Instruction flow for interrupt with register	Cost	of
TBCCR1	μΑ	cycles
TBCCR1 TBCCR1_ISR push R11 push R12 bit.w #BITB,R4. jnz Basic_P Basic_P add.w R7,&TBCCR1 bis.b #BIT4,&P1IE bic.b #BIT0,&P2IE Set_Vout bic.b #BIT1,&P2OUT bis.w #BIT2,&TBCCTL2 bis.w #BIT2,&TBCCTL3 bis.b #BIT1,&P5OUT jmp End_BP End_BP pop R12 pop R11	342 342 336 339 334 337 336 337 337 337 337 337 342 342	03 03 03 02 02 04 05 04 04 04 04 04 04 04 04 04 02 02 02 02
jmp TBX_ISRI	342 361	02 02

 TABLE IV

 Pulse Width interrupt instruction set

Instruction flow for interrupt with register TBCCR2	Base Cost μA	Number of cycles
TBCCR2_ISR mov.w TBCCR1,&TBCCR2 add.w R8,&TBCCR2 bic.w #BIT2,&TBCCTL2I	330 334 336	04 04 02

TABLE V REFRACTORY PERIOD INSTRUCTION SET

Instruction flow for interrupt with register TBCCR3	Base Cost μA	Number of cycles
TBCCR3_ISR mov.w &TBCCR2,&TBCCR3 add.w R9,&TBCCR3 bic.w #BIT2,&TBCCTL3 bit.b #BIT4,&P1IN jnz CompOffMag bis.b #BIT1,&P2OUT bit.w #BITB,R4 jnz CompOffMag bis.b #BIT0,&P2IE bic.b #BIT0,&P2IFG	330 334 336 339 337 336 339 337 336 339	04 04 05 02 04 02 02 02 02 02 04 04

TABLE VI INSTRUCTION SET FOR ECG INTERRUPT

	Base	Number
Instruction flow for interrupt with register	Cost	of
TBCCR4	μΑ	cycles
add.w R15,&TBCCR4 ;	334	04
bis.b#BIT0,&P6SEL	337	04
mov.w#ADC12ON+SHT0_2,&ADC12CTL0	330	05
mov.w #SHP,&ADC12CTL1	330	05
mov.b #SREF_2,&ADC12MCTL0	330	05
bis.w #ENC,&ADC12CTL0	337	04
bis.w #ADC12SC,&ADC12CTL0	337	04
bit.w #BIT0,&ADC12IFG	336	04
jz testIFG	339	02
mov.w &ADC12MEM0,EGMstart(R10);	330	06
add.w #2,R10	334	01
add.w #2,EGMCurrent	334	04
bic.w #BIT0,&ADC12IFG	336	04
bic.w #ADC12ON,&ADC12CTL0	336	05
bic.b #BIT0,&P6SEL	336	04
bis.b#BIT0,&P6DIR	337	04
cmp.w #14000,EGMCurrent	338	05
jlo END_ADC	336	02
END_ADC jmp TBX_ISR	361	02
- *		





Fig.10. Average Current distribution of interrupts

For the basic pacing rate of 74 bpm, the time interval is 60000/74 bpm = 0.8 sec. When, interrupt execution, takes current of $335.162 \ \mu$ Amp. to generate a pulse width of $1.50 \ msec.$ to stimulate heart the average current will be $2.62 \ \mu$ Amp. i.e. $2 \ \mu$ Amp is LPM3 mode standby current and $0.62 \ \mu$ Amp is the current addition in 0.8sec. Other interrupt adds approximately 0.62 $\ \mu$ Amp current in every 0.8 sec. too. Hence average current consumption in this interval is 4.48 \ \muAmp.as shown in figure 10.

VI. RESULT AND CONCLUSION

Pacemaker is a very crucial low power device. Software design using internal peripherals for its various functionalities such as Basic Pacing, Pulse width, Refractory period and ECG interval, is tested with respect to current consumption. Software and processor peripherals are used to generate pulse to stimulate heart. This consumes less current, thereby leaving a margin for external hardware. For MSP 430F1612, in LPM3 mode standby current is 2 µA. For the four interrupt handlers as shown in table III, IV, V and VI has an estimated current 339.723 µAmp, 332.8 µAmp., 335.757 µAmp and, of 335.162 µAmp respectively. Average current is 4.48 µAmp., which is calculated according to the method given in figure 5. Though, this is for only the limited pacemaker parameters, strategy seems to be useful to increase the battery life as given in equation 2. The work is aimed towards development of a reliable methodology to design a power crucial low cost biomedical instrument.

VII. REFERENCES

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