Simulation of Various SOI Models at Nanometer Technology

Nisha Doshi, Laxman Pai, Rajesh Bhole, Kiran Purabia and S. S. Rathod

Abstract-- **Silicon on Insulator is very attractive technology for large volume integrated circuits production and is particularly good for low voltage, low power and high speed digital systems. The performance advantages associated with SOI hence led to consideration of the technology for high performance applications such as microprocessors, digital signal processors and wireless applications.**

Even the simplest integrated circuit design begins with circuit simulation. This requires accurate models and simulators. SOI simulation being relatively new is still being optimized to make it as robust as bulk models. SOI has resulted in the generation of an entirely different set of modeling problems when compared to bulk. Most early versions of major simulators are not very comparable with SOI simulations especially in the nanometer regime. It is necessary to access performance and reliability of different SOI models at the submicron technology node.

This paper compares various types of available SOI models by simulating the characteristics. Both Matlab and T-spice simulations are carried to compare performance of models in the nanometer technology and results are presented in the paper.

***Index Terms*-- MOSFET, BSIM, SOI, TCAD, Device Model.**

I. Introduction

SILICON on Insulator technology has been becoming an important technology for deep submicron CMOS VLSI. SOI CMOS technology has been regarded as another major VLSI technology in addition to bulk CMOS technology. VLSI circuits using SOI CMOS technology have been reported increasingly as shown in fig. 1. Using deep submicron SOI technology, various VLSI circuits including DRAM, SRAM, logic circuits and gate arrays have been integrated. As compared to the bulk CMOS circuits, SOI CMOS circuits have a better speed performance owing to smaller parasitic capacitances. As a result, higher-speed low power applications can be obtained [1, 5].

Since the performance of SOI CMOS devices is quite different from that of the bulk ones, models designed for bulk CMOS devices may not be sufficient for circuit simulation. There are lots of models provided for the SOI technology for device size ranging in the microns. But for the nanometer technology verification and applicability of the models need to be checked in the submicron domain. In advanced deep-submicron CMOS technologies especially for integrating memory circuits, narrow channel and short channel effects are important in determining the device performance. In addition sidewall conduction of narrow channel SOI CMOS devices can not be neglected.

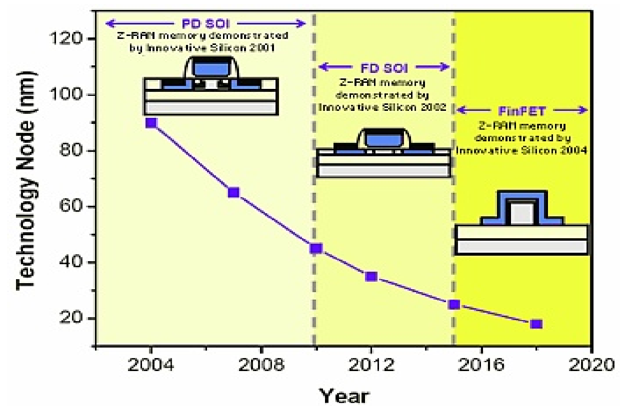

Fig. 1. Technology generation representing SOI is leading in the research with reduction in the device size (Source: Innovative Silicon website)

Furthermore, when channel length is very small, electron temperature effect is also important. Under this situation available models may not be applicable in submicron region. Accuracy of the device model is critical for determining the precision of the result. This paper describes the analytical device models of deep submicron fully depleted SOI CMOS devices. It will be shown that as verified by spice simulation consideration of the models is important for deep submicron fully depleted SOI technology.

II. SOI Technology Models

Various models like BSIM, threshold voltage, subthreshold current and mobility and strong inversion model are considered. The models are described in the following subsections.

A. BSIM Model

Spice CMOS device models have been continuously improved in the past. In late 1980's, BSIM model announced Level 1 model, which is also called Shichman-Hoges model,

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is suitable for MOS device with a channel length of greater than 2μm. Level 2 model, which is suitable for MOS devices with a channel length greater than 2μm, already includes the second order effects including the lateral and vertical electric field dependent mobility model [6].

Cutoff region: $V_{gs} \leq V_{th}$: $I_d = 0$ (1)

Linear region: $V_{gs} > V_{th}$ and $0 < V_{ds} < V_{d,sat}$:

$$I_{ds} =(\mu_0/(1 + U_0(V_{gs} - V_{th})))*(C'_{ox}*W_{eff}/L_{eff}) / (1+U_1/L_{eff}*V_{ds}) ((V_{gs} - V_{th})V_{ds}-(a/2)*V_{ds}^2) \quad (2)$$

Saturation region: $V_{gs} > V_{th}$ and $V_{ds} \geq V_{d,sat:}$

$$I_{ds}= \mu_0/(1 + U_0(V_{gs} - V_{th}))* C'_{ox}*(W_{eff}/ L_{eff}) /2aK* (V_{gs} - V_{th})^2 \quad (3)$$

B. Threshold Voltage Model

This model models the threshold voltage of a small geometry SOI MOS device. Threshold voltage model considers short-channel and narrow-channel effects. This model can well predict the body effect and the small geometry effect. The model equations for threshold voltage model are as shown in equation 4, 5, 6 and 7 for centre as well as sidewall region. It considers short channel and narrow channel effects [6].

For Center-Channel Region:

$$V_{TH,c} = V_{FB}+\Phi_G-\Phi_{si} \quad (4)$$

$$\phi_G = (-\phi_{si}*(1+C_{si}/C_{ox1}+C_{ox2}) - \phi_3*(C_{si}/C_{ox1})*(1-\delta_2) - (E_0/2q)*(C_{si}/C_{ox1})*\delta_3 + (q*N_{si}*t_{si}^2) * (C_{si}/C_{ox1}) * (1+2C_{si}/C_{ox2}) * (1-\delta_1)/(2\varepsilon_{si})) / (1+C_{si}*(\delta_2-\delta_3) / C_{ox1}+C_{si}/C_{ox2}); \quad (5)$$

For Sidewall Region:

$$V_{TH,s} = V_{FB} + \phi_G - \phi_{si} ; \quad (6)$$

$$\phi_G = (-\phi_{si} + \delta_{1,s} * (q * N_{si} * l_o^2/\varepsilon_{si}) - \delta_{2,s} * \phi_{s3} + \delta_{s,3}*E_o/2q) / (1-\delta_{2,s}+\delta_{3,s}) ; \quad (7)$$

C. Subthreshold Current Model

When the gate-source voltage (V_{GS}) is smaller than the threshold voltage- the subthreshold region, diffusion dominates in the device. This model depends majorly on tsi, Nsi and channel length L [2, 3, 4, 6]. Therefore, the diffusion current of the center channel used is

$$I_{diff,c}=I_1 * (W/L)) * (1-\exp(-V_{ds}'/ (kT/q))) * (\exp((V_{gs}'-V_{ths}) / (n_c* kT/q)) / (1+ \exp((V_{gs}'- V_{ths}) /(n_c* kT/q)))); \quad (8)$$

The diffusion current of the sidewall channel region,

$$I_{diff_s}=I_2* (1/L) * (1-\exp(-V_{ds}'/ kT/q)) * (\exp((V_{gs}'-V_{ths}) / (n_s* kT/q)) / (1+ \exp((V_{gs}'-V_{ths}) /(n_s* kT/q)))), \quad (9)$$

Where I_1 is a scaling coefficient, I_D is the total drain current, R_S and R_D are the parasitic resistances of the source and the drain, respectively. VJ is the slight potential barrier between the source/drain and the channel.

D. Mobility and Strong Inversion Current Model

When the channel of a fully depleted SOI CMOS device is very short, the electron temperature effect can not be neglected. An electron temperature dependent mobility model is referred to the difference between the electron temperature and the lattice temperature. This model describes mobility and strong inversion current of an SOI CMOS device in terms of Triode and Saturation region. It considers impurity scattering, surface scattering, velocity overshoot phenomenon and electron temperature effect [6].

The equation 10 represent low field mobility at lattice temperature, equation 11 represents effective mobility of center channel region and equation 12 represents surface mobility of center channel.

$$\mu_o(T_L) = \mu_o(T_o)*T_o^2/T_L^2 ; \quad (10)$$

$$\mu_{eff,c}(V_{DS}')=4*\mu_{s,c}/(3+(1+p*V_{DS}'^2*\mu_{s,c}^2)^{1/2}) ; \quad (11)$$

$$\mu_{s,c} = \mu_o(T_L)/[1+\theta(V_{GS}'-V_{TH,c})] ; \quad (12)$$

The drift current in the center channel region,

$$I_{drift,c} = \mu_{eff,c}(V_{DS}') * C_{ox1} * (W/L) * [(V_{GS}'-V_{TH,c}) * V_{DS}'- 0.5*\alpha_{0,c}*V_{DS}'^2] ; \quad (13)$$

$$V_{Dsat,c} = V_{Dsat1,c} + V_{p,c} - (V_{Dsat1,c}^2+V_{p,c}^2)^{1/2} ; \quad (14)$$

$$E_{1,c}=-(2-\eta_1)*V_{Dsat,c}/L \quad (15)$$

The equation 16 represents effective mobility of center channel region and equation 17 represents surface mobility of center channel.

$$\mu_{eff,s}(V_{DS}') = 4*\mu_{s,s}/(3+(1+p*V_{DS}'^2*\mu_{s,s}^2)^{1/2}) ; \quad (16)$$

$$\mu_{s,s} = \mu_0(T_L)/(1+\theta*(V_{GS}'-V_{TH,s})) ; \quad (17)$$

The drift current in the sidewall channel region,

$$I_{drift,s} = \mu_{eff,s}(V_{DS}') * 2 * (C_e+C_{sw}*t_{si}) * [(V_{GS}'-V_{TH,s}) * V_{DS}'- 0.5V_{DS}'2]/L \quad (18)$$

$$V_{Dsat,s} = V_{Dsat1,s} + V_{p,s} - (V_{Dsat1,s}^2+V_{p,s}^2)^{1/2} ; \quad (19)$$

$$E_{1,s}=-(2-\eta_1)*V_{Dsat,s}/L \quad (20)$$

III. RESULTS AND DISCUSSION

The above model equations are simulated in Matlab [7, 8]. The models are also developed in visual C++ and then these models are given to the T-Spice to compare the performance of mathematical model and the circuit simulation. All the models are verified at submicron technological nodes e.g. 32nm, 65nm and 90nm.

Fig. 2 shows the plot of BSIM model and found that drain current increases with the reduction in the device size. At 32nm it is clear from the profile that due to impact ionization, saturation current increases rapidly.

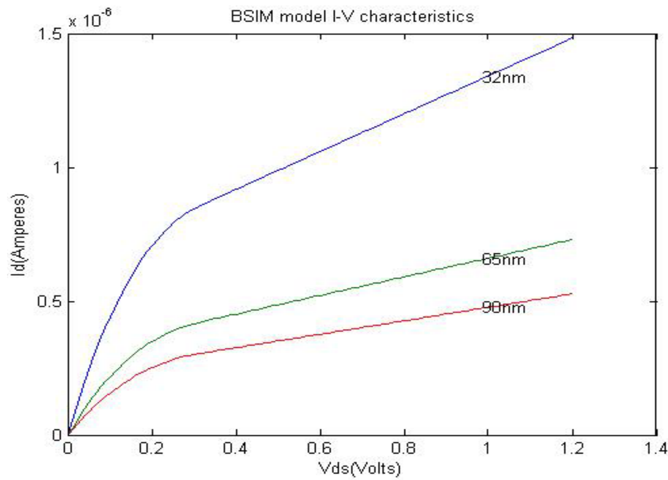

Fig. 2. I-V Characteristics of BSIM

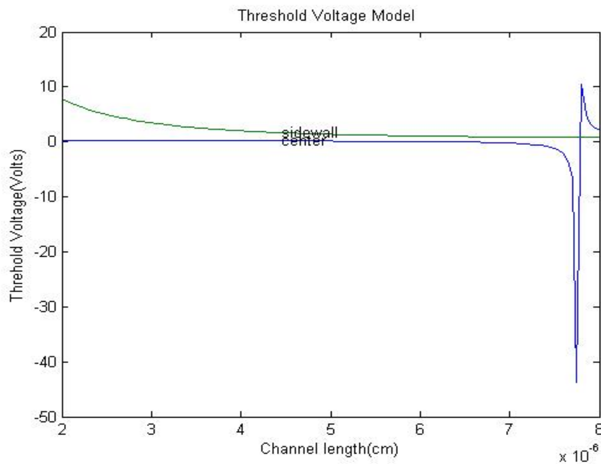

Fig. 3. Plot of Threshold Voltage Model for 20nm to 80nm

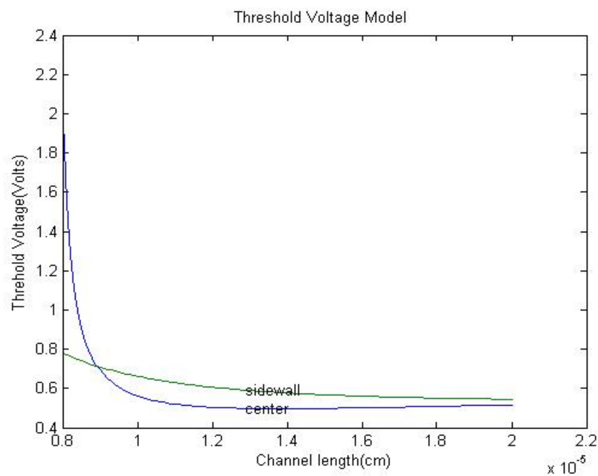

Fig. 4. Plot of Threshold Voltage Model for 80nm to 220nm

Fig. 3 and fig. 4 shows the plots of threshold voltage model and found that threshold voltage changes with change in the device size up to 78nm properly. But when device size is less than 78nm then mathematical model does not give the correct result and there is sudden change in the threshold voltage is observed. The intersection of sidewall and centre profile shows the threshold voltage of the device and found to be o.7V from fig. 4.

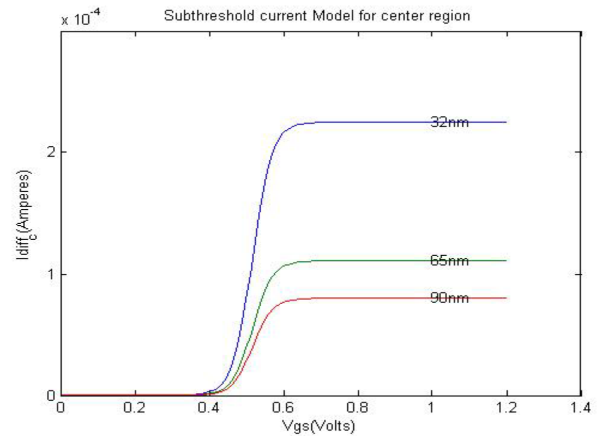

Fig. 5. Plot of Subthreshold Current Model for Centre Channel Region

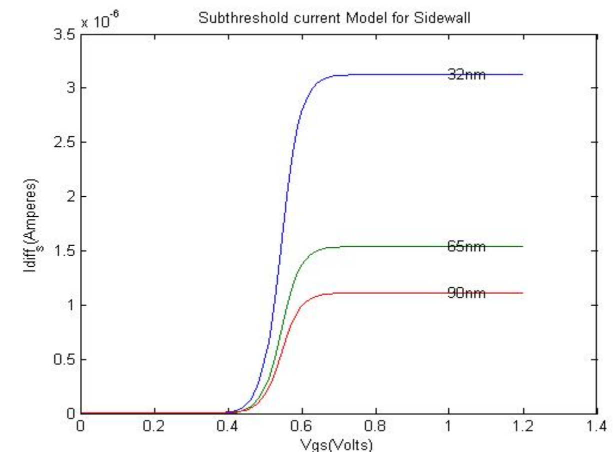

Fig. 6. Plot of Subthreshold Current Model for Sidewall Channel Region

Fig. 5 and fig. 6 shows the plots of sub threshold current voltage model for centre channel and sidewall channel and found that the model works properly in the submicron region. The sub threshold current is found to increase with the reduction in the device size.

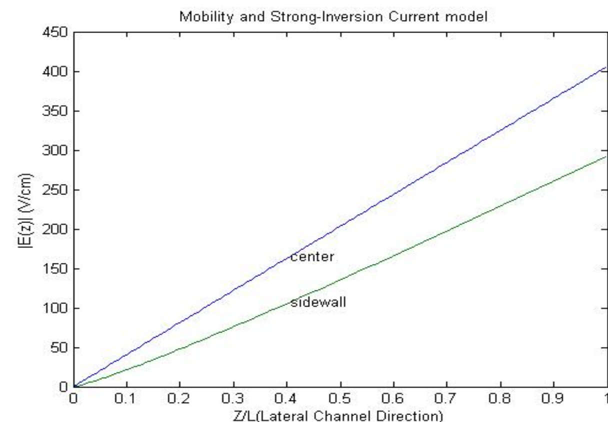

Fig. 7. Plot of Mobility and Strong Inversion Current Model

The plot for mobility and strong inversion current model is shown in fig. 7 and found that electrical field profile in the centre channel region is larger than that in the sidewall channel region.

IV. Conclusions

We have simulated SOI models analytically for 32nm, 65nm and 90nm technological node and found that these models need to be reconsidered for 65nm and 32nm technological node. BSIM model gives rise rapid change in the saturation mode current when technology reaches to 32nm and thus that factor should be accounted in the model. Threshold model also gives abrupt change in the threshold voltage at 78nm technological node and hence modification of this model for 78nm technology and less is necessary.

V. Acknowledgment

The authors gratefully acknowledge the facilities provided in VLSI Laboratory of Electronics Engineering Department, Sardar Patel Institute of Technology, Mumbai.

VI. References

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VII. Biographies

Nisha Doshi was born in Mumbai in India on 1986. She is graduate student of Sardar Patel College of Engineeriing, Mumbai. Her area of interest is Microelectronics and VLSI Design. She won prize at state level project presentation in 2004.

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