Low Power SRAM Design Using T-Cell

Ronak Gandhi and S. S. Rathod

Abstract—**Basic 6-transistor T-Cell for structure SRAM SOI (Silicon on Insulator) cell is proposed. The structure gives an added advantage to conventional cell in terms of power dissipation. It also improves area and simplifies process parameters which are simulated on tools like Tanner EDA and Microwind. The structure is simplified and save space and power. Furthermore the SRAM structure is compared on different models available e.g. BSIM4, LEVEL-1 and LEVEL-3 and comparison is made within these models on MOS characteristic.**

Index Terms—**T-Cell, SOI, Low Power, 6-T SRAM, MOS**

I. Introduction

THE SOI cell technology is widely used in IC manufacturing. Its performance is merited with lower power dissipation, low noise, high rejection to radiation and negligible latch-up effect in contrast to existing conventional CMOS devices [1]. Using deep submicron SOI technology, various VLSI circuits including DRAM, SRAM, logic circuits and gate arrays have been integrated. SOI CMOS technology has been used to implement low power SRAM, multi-giga-bit DRAM, 1 GHz microprocessors, and other high-speed low-power computer-related VLSI circuits.

The published paper by Sug Hun Hong et. al. [2] described a novel T-shaped shallow trench isolation (STI) technology, which has the same effective isolation length with conventional STI but significantly reduced aspect ratio. The T-shaped STI was formed using 2-step trench etches. After the formation of the 1st trench of a relatively low aspect ratio, oxide spacer was formed inside the trench sidewall. And the 2nd trench was made to ensure an effective isolation length. When T-shaped STI was filled with undoped silicate glass (USG) and high density plasma (HDP) oxide, the mouth of 2nd trench is closed by the overhang of filling materials so that the effective aspect ratio of T-shaped STI can be lowered. T-shaped STI shown comparable characteristics to conventional STI and no electrical or physical degradation was found.

A four transistor static random access memory (4T SRAM) cell and a silicon-on-insulator dynamic random access memory (SOI DRAM) gain cell, both operating at low supply voltage, was proposed by Mamoru Terauchi [3]. Both cells actively exploit the body region of partially depleted SOI MOSFET's. The body region of an SOI MOSFET with an `H-shaped' gate electrode was used as a resistor in the inverter pair of the SRAM cell. Its resistance was controlled independently from the threshold voltage of the main MOSFET. Published result shows the stable operation of the proposed SRAM cell under a low supply voltage.

This is an attempt to resent study carried on in field of Microelectronics especially in T-Cell technology. The T-Cell is applied to static RAM and analysis for various parameters using different models is carried out. Section II describes the basic T-Cell structure and 6-T SRAM cell using proposed T-Cell structure for MOSFET and finding are discussed in section III.

II. T-Cell Structure and SRAM Design

The layout of nMOS T-Cell is as shown in fig. 1. T-Cell is formed on a main surface of a semiconductor substrate with T-shape polysilicon intersecting with an active layer. Metal contact is established at one of the terminal of polysilicon. This structure has two substrate terminals that greatly enhance the performance of structure. The width of the laid polysilicon is reduced as compared to the conventional structures due to this the resistivity of the device increases. This tends to reduce the current in the structure and hence the power dissipation.

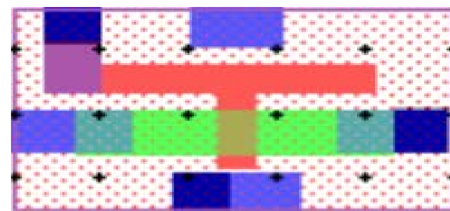

Fig. 1. Basic Structure of T-Cell for nMOS

The schematic diagram for 6T-SRAM [4, 5] in data reading state is as shown in fig 2. Transistors M3 and M4 are the access transistors and M1, M2, Mp1 and Mp2 forms the basic latch structure of SRAM. Transistor M5 and M6 are used to drive the sense lines. For all the transistors one of the substrates is tied to the ground while other is applied to Vdd. Layout for this SRAM cell using proposed T-Cell structure is designed using L-Edit and is as shown in the fig. 3.

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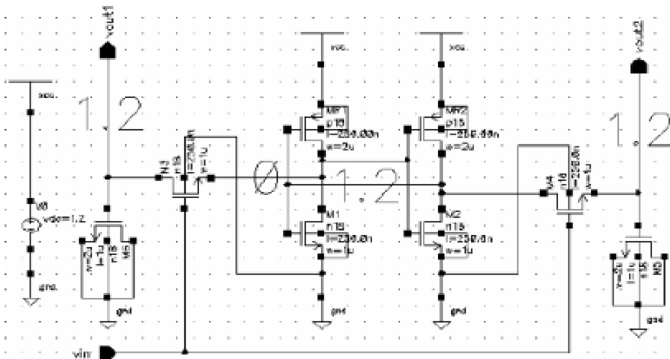

Fig. 2. Schematic Diagram for 6T-SRAM in data reading state

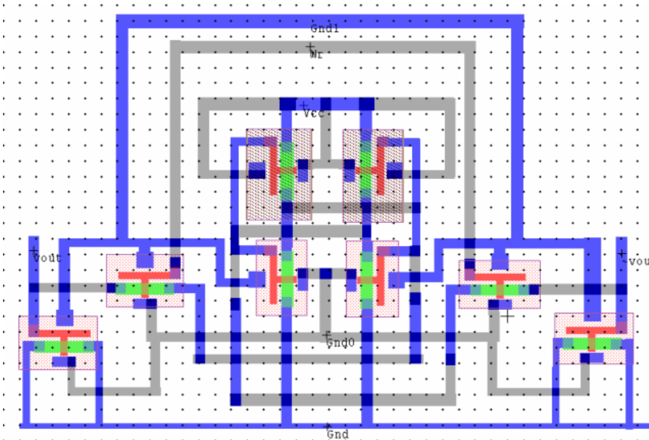

Fig. 3. Layout for 6T-SRAM in L-Edit

III. Results and Discussion

Various MOS parameter and simulation values are listed in TABLE-I. These parameters are used for simulation using T-Spice [6] of MOS characteristic of T-Cell for different simulation algorithm.

TABLE I
VARIOUS PARAMETERS CONSIDERED FOR THE MOS CHARACTERISTICS

Parameter	**BSIM4**	**Parameter**	**LEVEL-3**
VTHO	0.400	VTO	0.70
K1	0.500	LD	0.00
K2	0.000	U0	0.060
TOXE	3.000	TOX	3.000
DVT0	2.200	PHI	0.68
DVT1	0.530	GAMMA	0.35
LPE0	23.000	KAPPA	0.01
NFACT	1.000	THETA	0.35
PSCBE1	500.000	VMAX	130.00
U0	0.067	NSS	0.05
UA	1.000		
UC	-0..047	**Parameter**	**LEVEL-1**
VSAT	80.000	VTO	0.70
PCLM	1.200	U0	0.060
LINT	0.000	TOX	3.000
WINT	0.000	PHI	0.68
KT1	-0.110	GAMMA	0.35
UTE	-1.500	Parameter	LEVEL-1
VOFF	0.050		

Fig. 4, 5 and 6 shows the plot for Voltage Vs current across drain to source (Vds vs Ids) of the Cell. The results indicate that the ohmic region is maximum for BSIM4 and is minimum for LEVEL3. Oxide breakdown is much higher for BSIM4 as compared to the other models. These results are obtained with the proposed T-CELL for SRAM.

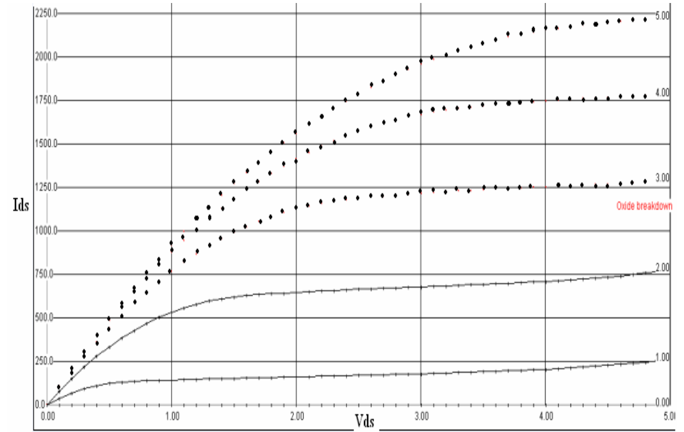

Fig. 4. Plot for BISIM4 Vds vs Ids for different values of Vgs

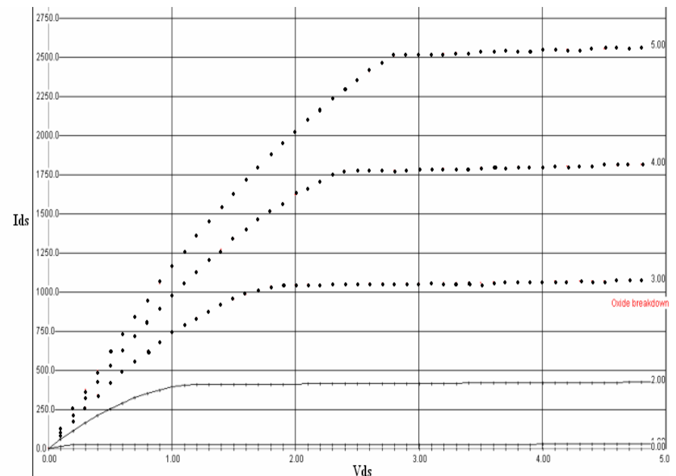

Fig. 5. Plot for LEVEL1 Vds vs Ids for different values of Vgs

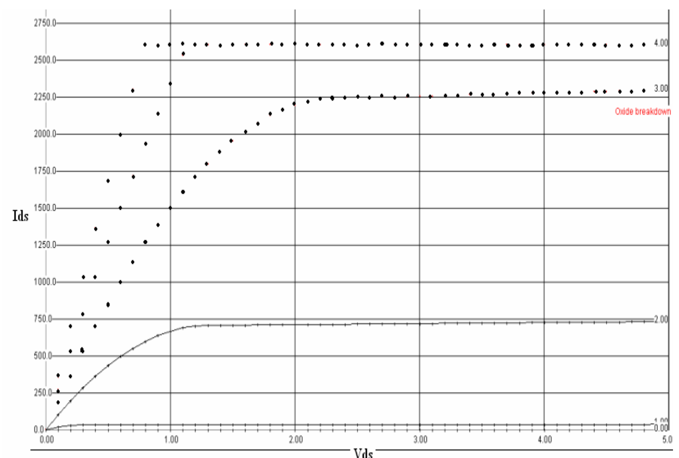

Fig. 6. Plot for LEVEL3 Vds vs Ids for different values of Vgs

Results obtained for response of Vgs to Ids as shown in fig. 7, 8 and 9, reflects that the threshold voltage is lower for BSIM4 as compared to that of LEVEL1 and LEVEL3.

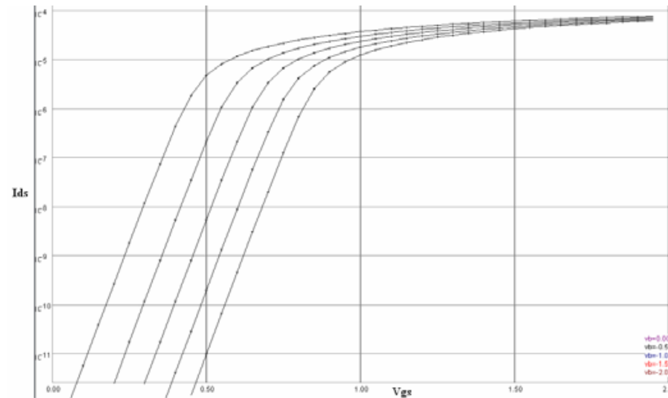

Fig. 7. Plot for BISIM4 Vgs vs Ids for different values of Vb

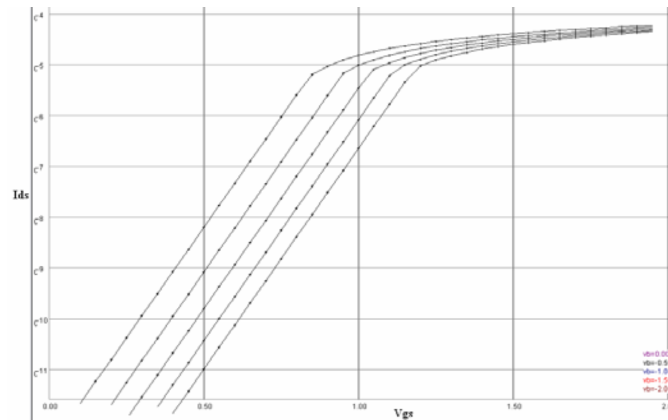

Fig. 8. Plot for LEVEL1 Vgs vs Ids for different values of Vb

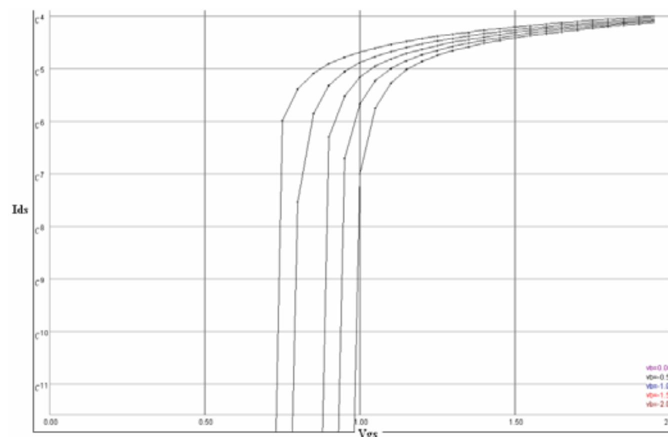

Fig. 9. Plot for LEVEL3 Vgs vs Ids for different values of Vb

Figure 10 indicates output waveform for proposed 6-T SRAM implementation using T-Cell and found that proposed 6T-SRAM cell works properly if designed using T-Cell. The waveforms are for the data write operation to the cell and found that data is correctly written to the cell. Fig 11 shows the transient response for input voltage vs time and current for inverter vs time. The results produced shows that the current while writing to the cell is very less. The structure gives less writing delay and consumes less power as compared to the conventional techniques used for designing the SRAM.

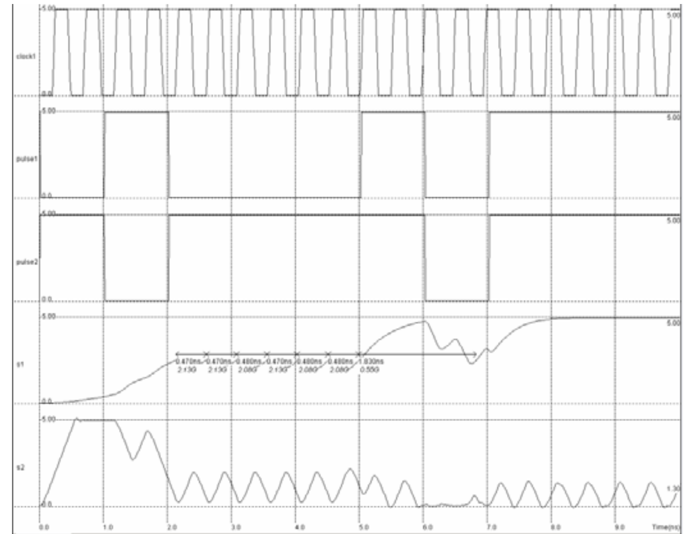

Fig. 10. Simulation Waveforms of proposed SRAM T-Cell

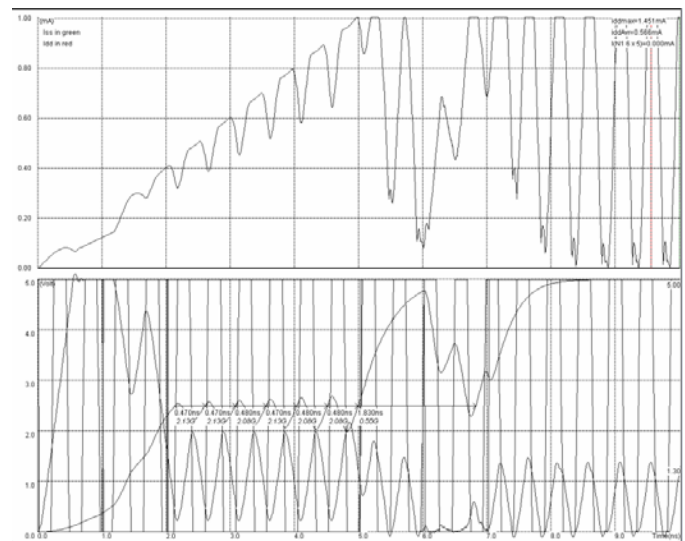

Fig. 11. Plot for Voltage Vs time (lower) and current Vs time (upper) of proposed SRAM T-Cell

IV. Conclusions

The design of SRAM using T-Cell ensures that the SRAM functions properly under different operating conditions. Transfer speed and power dissipation is analyzed for different models by comparing the proposed structure and conventional structure and found to improve with the proposed structure. Considering the extremely low power dissipation, the small area of the cell as well as the advantages of SOI, this design is prominent and prospective when device is scaled down.

V. Acknowledgment

The authors gratefully acknowledge the facilities provided in VLSI Laboratory of Electronics Engineering Department, Sardar Patel Institute of Technology, Mumbai.

VI. References

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VII. Biographies

Ronak Gandhi was born in India, Mumbai on May 21,1985. He completed his Batchlor of Engineering in Electronics from Sardar Patel college of Engineering, Mumbai(India), Diploma from Thakur Polytechnic in Electronics and Communication Engineering,Mumabai and schooling from St.Francis D'Assisi High School,Mumbai

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Ronak recieved many awards for paper presentation and project at state level. He also lots of project under his credits and wish to work on research project and also wish to contribute his knowledge sharing skills but also wish to work for the betterment of humanity from technical skill set.

S. S. Rathod (M’2007) was born in Amravati in India on Feb 28, 1975. He graduated from the College of Engineering Badnera, and completed his post graduation in the field of Electronics Engineering from V.J.T.I., Mumbai-India. Currently he is pursuing his doctoral research at Indian Institute of Technology, Roorkee-India.

His employment experience includes eight years as an educationalist. He has published more that 20 papers in various national and international conferences. His special fields of interest include VLSI Design, process and device modeling. His name is listed in the science category of Marques Who’s Who USA. He received outstanding achieving ward by the Energy Society, India. He is member of IEEE, ISTE and ISNT.