Design of Low Power Integrated SAR-ADC in 0.18µm Mixed-Mode CMOS Process

Aniruddha C. Kailuke, Vrushali G. Nasre, M.Shojaei-Baghini, Rajendra.D.Kanphade *Member, IEEE*

Abstract- **Main building blocks of a SAR-ADC are: sample & hold circuit, comparator, timing and logic control which is mainly SAR logic, DAC (Digital to Analog Converter) in the feedback loop of ADC. For low-power applications designer needs to come up with a compromise among speed, resolution and speed. In this paper a SAR-ADC is designed in 0.18µm CMOS technology in such a way that the total power is minimized while medium sampling rate and 8 bit resolution are achieved. A passive sample-and-hold stage and a capacitor-based digital-to-analog converter are used to avoid use of current to voltage converter. This design is suitable for standard CMOS technology with low-power low-cost VLSI implementation. It is well applied when embedded into system-on-chip (SOC) circuit designs.**

***Index Terms*-Analog-to-digital converters (ADCs), CMOS analog integrated circuits, low power, low supply voltage, successive approximation.**

I. INTRODUCTION

TODAYS trend in mixed-signal ASICs leads to integration of Analog-Digital-Converters (ADCs) with complex digital circuitry on a single chip. ADCs are a key element in mixed-signal ICs. The SAR architecture has the advantage of low power consumption at medium speed and medium resolution. With the charge redistribution technique it is possible to use self calibration to increased accuracy beyond device mismatching limits. Compared with other popular types of ADC architecture, successive approximation register (SAR) ADC provides numbers of advantages. With only one comparator in the whole system, SAR can achieve the demand for low power consumption.

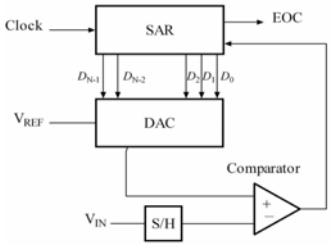

Fig. 1. Overall system Architecture of SAR-ADC

Aniruddha Kailuke is with the Department of Electronics And Telecommunication Engineering, Dept. DIMAT Raipur. (C.G.) INDIA (e-mail: anilkailuke@gmail.com).
Vrushali G. Nasre is with the Department of Electronics Engineering, Dept. BDCOE, Sewagram Wardha. (M.H.) INDIA (e-mail: vrushnasre@gmail.com)
Dr. M.Shojaei-Baghini is with the Electrical Engineering Department at IIT, Bombay, INDIA (e-mail: maryshojaei@gmail.com)
Rajendra.D.Kanphade is with the Department of Electronics And Telecommunication Engineering, Dept. SSGMCE, Shegaon. (M.H.) INDIA (e-mail: rdkanphade@gmail.com)

High resolution and accuracy can be achieved using capacitor array during data conversion. Considering these factors, SAR becomes an ideal component for some portable or battery-powered instruments. The overall system architecture is shown in "Fig.1". We designed and implemented all the blocks of SAR-ADC and results are validated using CADENCE Virtuoso Analog Design Environment IC (5.0.33/5.1.41) tool.

II. CONVERTER PRINCIPLE

Successive Approximation Converter based on a Charge Redistribution Principle is characterized in "Fig. 2". Binary weighted capacitors are used for the DAC. The switching point of the comparator is independent of the value of the input signal. During conversion, at the comparator input positive and negative voltages V_C referred to analog ground occur, whose magnitude is continuously decreasing with the number of conversion steps performed within a complete conversion cycle. Consequently, at the end of the conversion cycle, i.e., when highest precision is demanded, both comparator inputs are operated near analog ground [1].

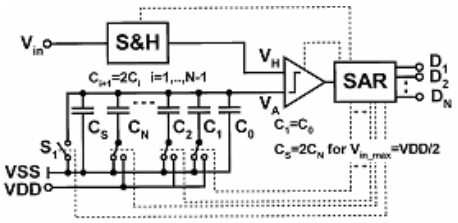

Fig. 2. SAR-ADC Based on a Charge Redistribution Principle

III. THE SAMPLE & HOLD CIRCUIT DESIGN

The Sample & Hold circuit is completely passive. It contains just a sampling switch, a dummy switch, a sampling capacitor and two clock buffers "Fig. 3". The passive S/H circuit gives a simple solution to the requirements of both small offset and wide input bandwidth of the SA-ADC to be used in an ADC array [2].

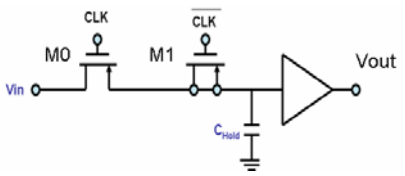

Fig. 3. Passive Sample & Hold Circuit

In this architecture "Fig.3", one dummy switch is used to minimize clock feed through error [3]. The theory behind this technique is that if the width of M1 is one half of M0 transistor, and clock wave form is fast enough then charge will cancel. The "Fig.4", shows the schematics of Sample and Hold circuit. The value of holding capacitor is 1pF.

Where transistor M0 operating in linear region, the condition for operating in linear region is

$$V_{GS} > V_T \tag{1}$$

$$V_{DS} < V_{DSAT} = V_{GS} - V_{TH} \tag{2}$$

$$I_{DS} = K' \frac{W}{L}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)V_{DS} \tag{3}$$

Where,

$K' = \mu_n C_{ox}$, V_{GS} = Gate Source Voltage,

V_{DD} = Supply Voltage, V_T = Threshold voltage

$$gm = \frac{K'}{2}\frac{W}{L}(V_{GS} - V_{TH}) \tag{4}$$

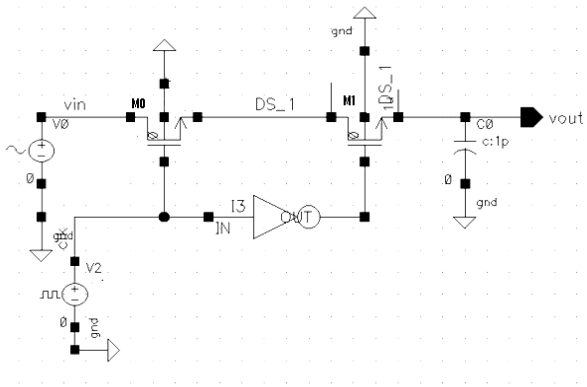

Fig. 4. Schematic of Sample-and –Hold Circuit

The calculated value of W/L for M0 & M1 is given in Table I The "Fig.5", shows the simulation result of S&H circuit "Fig.4".

TABLE I
ASPECT RATIO OF SAMPLE & HOLD CIRCUIT

Transistor	W	L
M0	2u	0.5u
M1	1u	0.5u

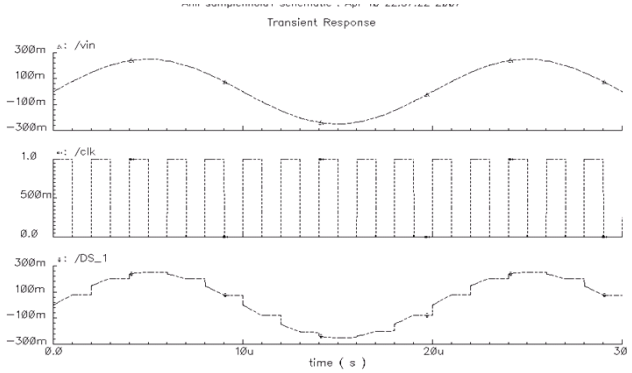

Fig. 5. Output Wave form for selected Sample-and Hold Circuit

III. CAPACITOR ARRAY DAC

The Binary weighted Capacitor DAC or Charge scaling DAC architecture is as shown in "Fig.6".In this architecture, a parallel array of the binary weighted capacitors is connected [3],[8]. The voltage output, V_{OUT}, can be expressed as relation (6)

$$V_{OUT} = KV_{REF}D \tag{6}$$

Where, V_{OUT} is the analog voltage output, V_{REF} is the reference voltage, K is a scaling factor and the digital word D is given by relation (7)

$$D = \frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \ldots + \frac{b_N}{2^N} \tag{7}$$

N is the total number of bits of the digital word, and bi is the i^{th} coefficient and is either 0 or 1. The relation (8) gives the value of V_{OUT} for any digital word.

$$V_{out} = \frac{Ceq}{(2C - Ceq) + Ceq} \times V_{ref} \tag{8}$$

Where, *Ceq* is the capacitors whose bits are set.

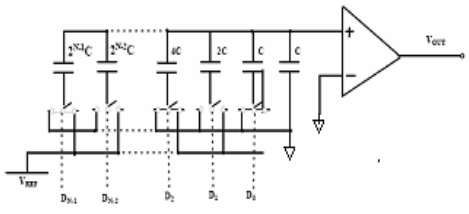

Fig. 6 Architecture of Charge Scaling DAC

We have implemented the architecture shown in "Fig.6" using CMOS capacitors and transistor switches as shown in "Fig.7", which is simulated using CADENCE Analog Design Environment. The values of capacitors C_{MSB}……..C_{LSB} are used as a multiple of unit capacitor of 20fF. Here we are assuming the unit capacitance is 20fF. The calculated values of all capacitors are given in Table II.

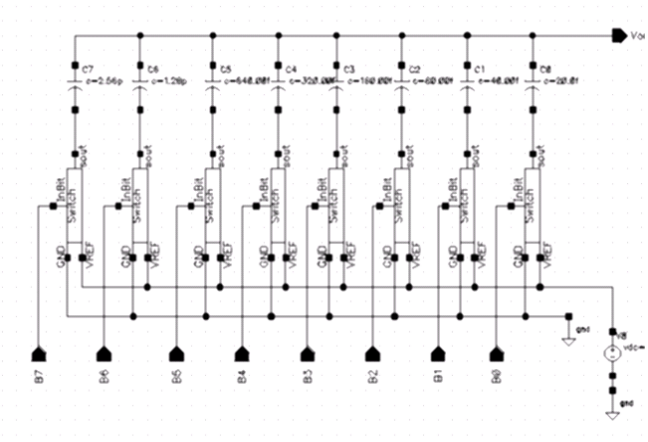

Fig. 7. Schematic of Charge scaling DAC

IV. DAC SWITCH DESIGN

This design is used to reduce charge injection and clock feed through errors by complimentary PMOS and NMOS switches shown in "Fig.8". All MOS transistors are operating in linear region [4],[5].

The "Fig. 8" shows a unit capacitor connecting to V_{REF} when bit-1 is set (High). Switch-1 PMOS, NMOS combination goes ON and connects to V_{REF}.

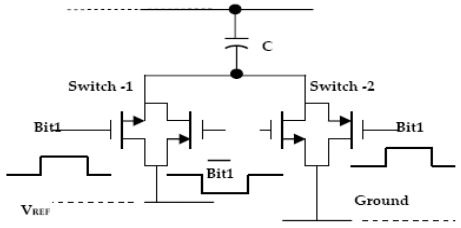

Fig. 8. DAC Switch architecture

Switch-2 PMOS, NMOS combination goes ON and connects to ground when bit-1 is reset [4],[6]. We have calculated the W/L of switch transistors and is given in Table II.

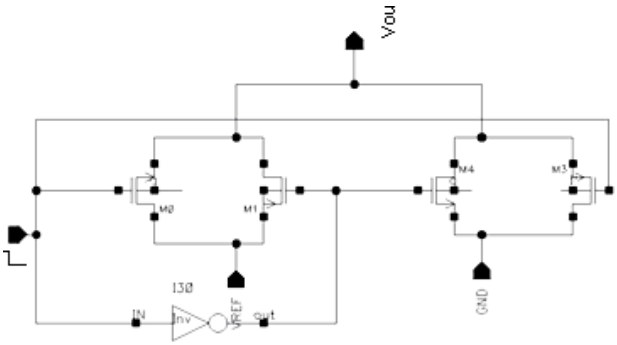

Fig. 9. Schematic of DAC switches

The "Fig. 9" shows implementation of DAC switch. The R_{ON} resistance of PMOS and NMOS transistor can be calculated using relation (9).

$$R_{ON} = \left[K' \frac{W}{L} \left(V_{GS} - V_T \right) \right]^{-1} \tag{9}$$

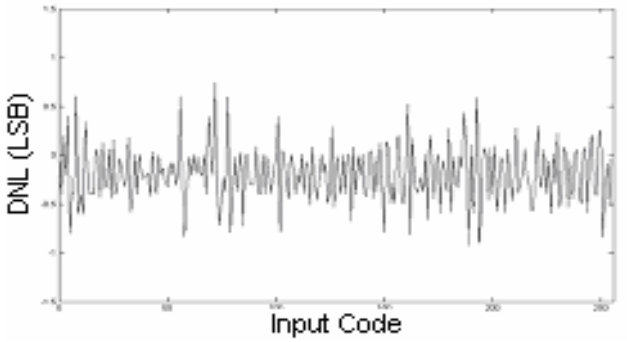

Fig.10 DNL plot for Charge Scaling DAC

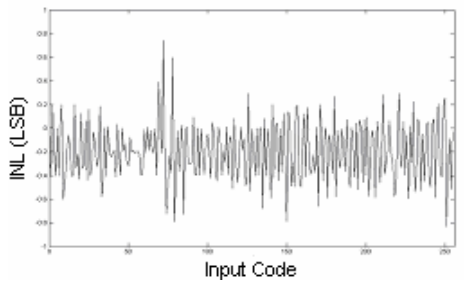

Fig.11 INL plot for Charge Scaling DAC

The Charge Scaling DAC is simulated in 0.18um CMOS process. The threshold voltages are 0.327 V for the nMOS and -0.4064V for the pMOS device. From "Fig.10", and "Fig.11", it is observed that a value of DNL is $\pm 0.7LSB$ and INL is $\pm 0.8LSB$ respectively.

V. COMPARATOR

The comparator is designed as a simple regenerative reset able circuit "Fig. 12", [1],[8] followed by inverters for signal level recovery. This type of comparator is use positive feed back bi-stable element to compare two signals. The advantage of this circuit is that there is no steady state power consumption. The only current will be the one required by bias circuit. The design approach is based on slew rate and optimum propagation delay constraints. Apart from offset related issues, the comparator is working as expected.

The bias current can be controlled by the bias transistor is as shown in "Fig.13", both transistor M2 and M3 is operating in saturation region and drain current of M2 and M3 can be given by equation (10)

$$I_{DS} = \frac{K'}{2} \frac{W}{L} \left(V_{GS} - V_{TH} \right)^2 \left(1 + \lambda V_{DS} \right) \tag{10}$$

We have assumed 2uA bias current to calculate the W/L ratio of the transistor M2 & M3. The aspect ratios of transistor M2 & M3 given in Table III. The complete schematic of comparator is as shown in "Fig.12".

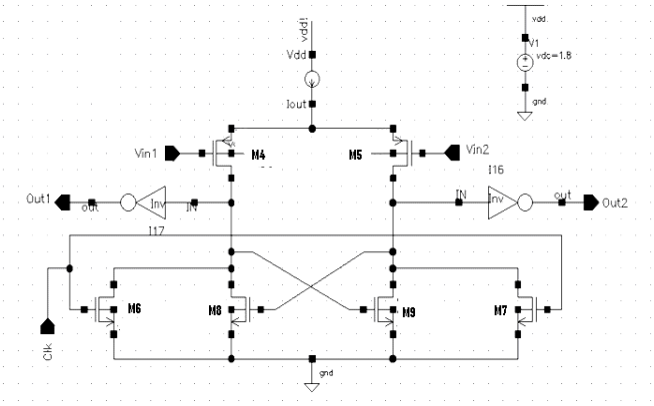

Fig. 12. Schematic of Regenerative Comparator

TABLE II
DAC SWITCHES SIZES AND ON RESISTANCES

For 0.18µm Technology								
Capacitor	C7 (MSB)	C6	C5	C4	C3	C2	C1	C0 (LSB)
Capacitor Value	2.56pF	1.28pF	640fF	320fF	160fF	80fF	40fF	20fF
NMOS/PMOS Switch Size in um	0.27/0.18	0.27/0.18	0.27/0.18	0.27/0.18	0.27/0.18	0.27/0.18	0.27/0.18	0.27/0.18
R_{ON} (NMOS)	2.04K	2.04K	2.04K	2.04K	2.04K	2.04K	2.04K	2.04K
R_{ON} (PMOS)	2.96K	2.96K	2.96K	2.96K	2.96K	2.96K	2.96K	2.96K

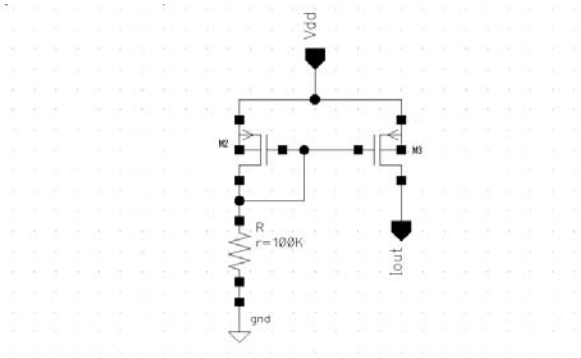

Fig. 13 Schematic of Biasing current source

The current I_D or bias current split in to I_{D1} and I_{D2} which flows through M4 and M5 respectively in differential pair transistor. This two current are depends on Vin1 and Vin2. Which can be expressed as relation (11).

$$I_D = 0.5I_D + 0.25K'\frac{W}{L}\Delta V\left(\frac{4I_D}{K'}\frac{W}{L} - \Delta V^2\right)^{\frac{1}{2}} \qquad (11)$$

Where $\Delta V = V_{in1} - V_{in2}$

The (regenerative) decision making circuit is the heart of any clock comparator where two pair of transistors are used for making decision.

TABLE III
TRANSISTOR SIZE

Circuit	**MOS**	**W**	**L**
Bias Current Source	M2	2u	0.4u
	M3	0.33u	0.4u
Differential Pair	M4	0.4u	0.18u
	M5	0.4u	0.18u
Switches	M6,M7	0.35u	0.18u
	M8,M9	0.27u	0.18u
Inverter	P_{MOS}	3u	0.18u
	N_{MOS}	1.23u	0.18u

The decision making circuit is as shown in schematic in "Fig.12". In the schematic both M6 and M7 are acting as a switch and this two transistor operating in linear region. And similarly transistor M8 and M9 is the heart of decision making circuit this two transistor are also operating in linear region the aspect ratio of this four transistor can be calculated by relation (3). Considering VDD=1.8V and maximum current 2uA.The calculated W/L is given in Table III.

The output stage of comparator is nothing but the inverter for high output impedance. The aspect ratio of inverter is also given in Table III.

The simulation result of comparator is given in "Fig.14", where Vin2 is used one Ramp signal as a input for simulation and Vin1 is as a fixed input. The simulation result clearly show that when Vin1> Vin2 and clock is low the Vout2 is low and when clock is high then Vout2 is always high. So we conclude that this comparator is working when clock is not present.

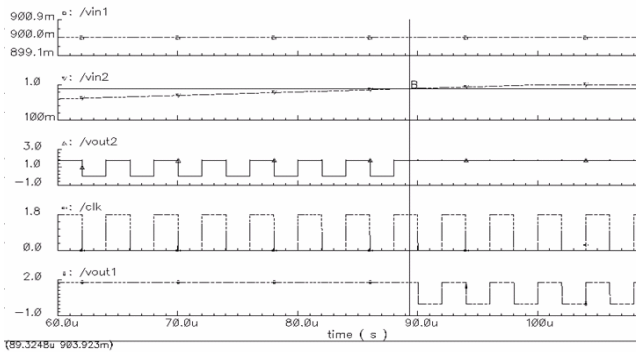

Fig. 14. Output waveform of Regenerative comparator

VI. SAR LOGIC DESIGN

A successive approximation register (SAR) is a digital control circuit, which is implemented using D flip-flop. We have designed D flip-flop using Verilog-A code. It has a parallel world output, which is connected to the input of an n-bit D/A converter. The input of the SAR is a one bit digital signal, which is taken from the output of the comparator. To start the conversion, MSB in the SAR is set to 1 and all the other bit are set to 0. If the input is higher than the output of DAC then MSB of the SAR is set to d0=1 other wise d0=0. The content of SAR is changed to [d0 1 0…….0] in the second step, and [d0 d1 1 0….0] in the third step. The procedure of the successive approximation is continued until the desired accuracy is reached. The classic SAR algorithm flow chart is as shown in "Fig. 15" and the logic diagram of successive approximation register is shown in "Fig.16".

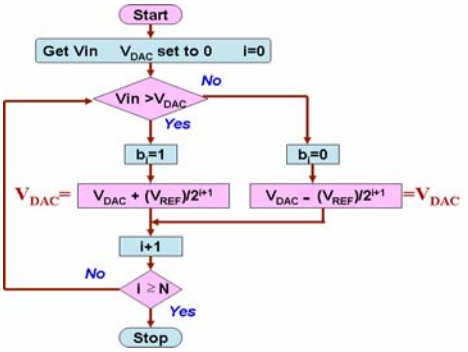

Fig. 15. SAR algorithm flow chart

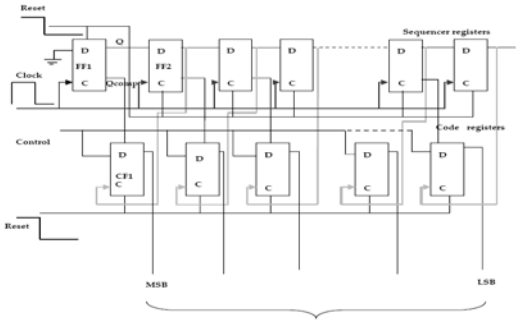

Fig. 16. logic diagram of successive approximation register

VII. CONCLUSION

A successive approximation converter suitable for operation at low supply voltage is designed in a standard 0.18um CMOS technology. We design all the building blocks of SAR-ADC using transistors with threshold voltages of approximately 0.327V for NMOS and – 0.4064 for PMOS. The simulation results indicate that the circuit achieves 8-bit monotonic conversion at high speed with differential nonlinearity less than 1 LSB. This device is suitable for standard CMOS technology VLSI implementation. These results are validated using CADENCE mixed signal Virtuoso Analog Design Environment IC (5.0.33/5.1.41) tool.

VIII. ACKNOWLEDGMENT

The work is supported by VLSI & Embedded Design Center SSGM College of Engg. Shegaon (M.S.), India.

IX. REFERENCES

[1] Jens Sauerbrey, Doris Schmitt-Landsiedel, Roland Thewes, "A 0.5V, 1µW Successive Approximation ADC", *IEEE Journal of Solid State Circuit, IEEE 2002.*

[2] Jiren Yuan and Christer Svensson," A 10-bit 5-MS/s Successive Approximation ADC Cell Used in a 70-MS/s ADC Array in 1.2-pm CMOS", *Ieee Journal Of Solid-State Circuits, Vol. 29, No. 8, August 1994.*

[3] David A. Johns and Ken Martin ,"*Analog Integrated Circuit Design*"2nd Ed. 2002 John Wiley & Sons(ASIA) Pvt. Ltd. Singapore.

[4] P. E. Allen, Holberg, *CMOS Analog Circuit Design* (New York Oxford Uni. Press.2004)

[5] Jens Sauerbrey, Doris Schmitt-Landsiedel, Roland Thewes, "A 0.5V, 1µW Successive Approximation ADC", *IEEE Journal of Solid State Circuit, IEEE 2002.*

[6] National Semiconductor Article – ABC's of ADC's by Nicholas Gray, November 24 2003.

[7] V. Peluso, P. Vancorenland, A. Marques, M. Steyaert, and W. Sansen, "A 900mV 40µW Switched Opamp ΔΣ Modulator with 77dB Dynamic Range", *ISSCC Digest of Technical Papers*, pp. 68-69, p. 414, 1998

[8] R. J. Baker, Li H. W., D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation* (IEEE Press)

X BIOGRAPHIES

Aniruddha C. Kailuke was born in India, on Aug 18, 1981. Currently he is pursuing M.E.(Digital Electronics) degree from the Department of Electronics and Telecommunication Engineering, SSGM College of Engineering, Shegaon SGB University, Amravati. He received BE from the Govt. College of Engg. Amravati. He has joined DIMAT, Raipur 2006 and is currently working as lecturer in the Department of Electronics and Telecommunication Engineering. His areas of research are VLSI and Embedded system Design and Analog and Mixed Signal Design.

Vrushali G. Nasre was born in India, on 25 Jan, 1983. Currently She is pursuing M.E.(Digital Electronics) degree from the Department of Electronics and Telecommunication Engineering, SSGM College of Engineering, Shegaon SGB University, Amravati. She received BE from the Bapurao Deshmukh college of Engg. Sewagram, Wardha. She has joined Bapurao Deshmukh college of Engg. and is currently working as lecturer in the Department of Electronics Engineering. Her areas of research are VLSI and Embedded system Design and Analog and Mixed Signal Design. Specially design of Data converter.

M. Shojaei-Baghini received M.S. and Ph.D. degrees in electronics engineering from the Sharif University of Technology, Tehran, Iran, in 1991 and 1999, respectively, where she was the first Ph.D. graduate in electronics. She received Post Doc. From IIT Bombay, in 2006.She was with the Emad Semiconductor Company where she was a Senior Analog IC Design Engineer. She has been Designer/Codesigner of several research/commercial analog and mixed-signal chips. She has also designed and successfully tested an ultralow-power signal conditioning chip for biomedical applications, and has worked on the impact of technology scaling on the behavior of digital synchronizers and CMOS technologies for analog/mixed-signal circuits. Dr. Shojaei was a corecipient of the third award on Research and Development at the 15th International Festival of Kharazmi in 2002. Her research interests include Analog/Mixed-signal/RF CAD tools, theory and implementation, Analog aspects of digital circuits, VLSI design and embedded systems. She is currently on the faculty of the Electrical Engineering Department at IIT, Bombay

Rajendra D. Kanphade is presently working as Incharge of "VLSI & Embedded System Design Center" of SSGMCE, Shegaon. He has joined SSGM College of Engineering, Shegaon in 1987. He has been Head of the Electronics Department for the period Oct 2003 to Jan 2006. He received B.E. (Electronics) degrees from SGB Amravati University, Amravati in the year 1987 & M.E (Electronics) from Dr. Babasaheb Ambedkar Marathwada University, Aurangabad in the year 1993. His areas of research are VLSI and Embedded system Design, Analog and Mixed Signal Design. Currently he is pursuing **Ph. D** degree from SGB Amravati University, Amravati. He is a member of IEEE, IETE and ISTE. He has published papers in journals and Conferences.