A Novel Approach to Automated Design of IC Layout Mask for Linear and Non-linear Structures Using LASI

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Abstract-- **The paper describes the design and implementation of a novel algorithm that enables the automated generation of TLC files for mask design using LASI. The algorithm accepts the dimensions of objects and their distances from axes as inputs and generates series of objects whose dimensions and separation distances are varied according to some functions specified by the user. The time and space complexity of the algorithm has been analyzed and estimated to be O(MN+R) and O(MN+Rn) respectively, where M types of boxes each of N numbers and R numbers of paths (polylines) each of n sides are drawn. The software tool that has been developed using the algorithm has been successfully applied to the layout design of MEMS based pressure sensors and also in the layout design of coplanar waveguide for RF MEMS applications.**

Index Terms-- **Algorithm, LASI, Layout Design, Piecewise Rectangular Approximation.**

I. Introduction

THE recent surge in the automation of VLSI design process with the aid of CAD tools demands creation and distribution of free softwares essential for chip fabrication. This motivated the design and implementation of a novel algorithm that enables the automated generation of files for mask design using LASI. The trend to replace boards with discrete electronic circuitry by a single application specific integrated circuit (ASIC) leads to the integration of both analog and digital functions on a single chip. However layout design for integrated circuits is a real challenge because of the scale of the problem: million of gates, complex interconnections of routed wires, complicated delay and timing interactions. However, because of the ASIC revolution in the past two decades, automated layout design is of great interest lately [1],[2]. IC layout mask design is the representation of an integrated circuit in planar geometric shapes corresponding to the top view of the layers that make up the various components of the integrated circuit and relative positioning of the mask layers for the actual fabrication process. It is one of the most important steps of both the full-custom and semi-custom IC design flow. Layout design greatly affects the performance of the resulting circuit since the geometry of the circuit determines the transconductances of the transistors, the parasitic capacitances and resistances. Also, the net silicon area needed is determined by the layout design. Layout design automation has been an interest of research over the last decade. Van Lierop proposed a bottom up approach for layout design automation [3]. Brück proposed a technology description language for analog and digital IC layout [4]. IC layout automation with analog constraints has also been a matter of consideration [8].

LASI (LAyout System for Individuals) is a freeware used for the purpose of layout designing. Contemporary literature reveals that a broad range of works have been done in the field of layout design. LASI has been used for layout design on Windows platform [5], [9]. It has been applied with digital standard-cell library using the MOSIS scalable design rules [6]. LASI has also been used as PC-based freeware CAD environment to design and tape out VLSI microelectronic circuits starting from schematic capture to a foundry compatible GDS II database [7]. The main difficulty in the process of layout drawing using LASI is that all the necessary co-ordinates of the different components of the mask design are to be calculated manually requiring a huge amount of time, energy and endurance. In this novel approach, programs in high level language (like C) are written in order to automate the whole procedure of creating TLC files for desired mask designs with all the required co-ordinates that are automatically calculated, thus enhancing the speed and alleviating the manual labor. This method is especially helpful when a large design with repetition of components of similar shape and size is to be implemented and also when the shapes and sizes of the components are varied according to some function. The proposed algorithm aims at designing the

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layouts of integrated circuits using boxes and paths. Moreover, the algorithm can be suitably applied to the design of non-linear structures like the tapered design of coplanar waveguides that can be used in RF phase shifter.

The paper is organized as follows: section II focuses on a brief overview of LASI. The idea of automated design of IC layout mask has been discussed in section III. Section IV emphasizes on the algorithm used to implement the automation process. The analysis of the algorithm is discussed in section V. Section VI discusses on the application of the tool developed using the algorithm to generate the .tlc files for the regular layout of MEMS based pressure sensor and the non-linear layout for the tapered design of a coplanar waveguide (CPW) for RF MEMS applications.

II. OVERVIEW OF LASI

'Layout System for Individuals' (LASI) is a free software meant for layout designing of ICs, MEMS, discrete devices etc. Drawing data is stored in text format making it easy to edit or add afterwards. All the layouts are drawn inside cells made of boxes, paths/polygons, texts and lesser rank cells. Boxes are objects having the properties of four sides, each orthogonal to the adjacent, and a layer. Path is a set of vertices in orderly form which is displayed as a set of endwise merged rectangles, all with the same width. A path with zero width is called a Polygon or Poly (usually called Polyline in other CAD tools). The cell information is stored in files with .tlc extension. TLC (Transportable LASI Cell) files are sequential files written in well documented form. TLC file, containing the information of a single cell, consists of Header Record, Object Record and Layer Record (optional). Under the Object Record, the co-ordinates and other parameters of the boxes or paths are to be specified in a predefined sequence. When the layout drawing window of LASI is opened, Cartesian axes are generated where the horizontal axis is the x-axis and the vertical one is the y-axis. For boxes, the sequence of specification is: layer number, bottom left x co-ordinate, bottom left y co-ordinate, top right x co-ordinate and top right y co-ordinate. For paths/polygons the order is: layer, width, number of vertices, x1, y1, x2, y2,…..,xn, yn. On the other hand, TLD (Transportable LASI Drawing) file is an extended TLC file format in a compound form containing a cell reference table, a layer table and other records of all the cells required to make a particular cell. At first TLC or TLD files are to be created by defining the boundaries of all the objects in the cell and then the files can be brought in the LASI drawing with the help of 'import' command. Thus LASI provides a PC based environment for layout designing.

III. THE IDEA OF AUTOMATED DESIGN OF IC LAYOUT MASK

The basic difficulty in the LASI drawing originates from the manual calculation of the co-ordinates of all the objects necessary for the design. This process is not only time consuming, but also it demands a lot of manual labor. It entails for the job of writing down the whole design in the predefined sequential format. The primary goal of the present work is to minimize this trouble by automating the complete system with the help of computer program. The program has been written in Turbo C. The program accepts the distances of the objects from the x and y axis and lengths and breadths of the objects as inputs. The turbo C program then creates a .tlc file and writes the x and y co-ordinates of necessary vertices of each object in the documented form along with all the records. The ultimate inevitability of the program is observed when the lengths, breadths and spacing of the component boxes are changing with some function. This task is easily done by a computer program with only the input of the length, breadth and initial spacing of the first box and the function which governs the change in those parameters of the following boxes. The only job of the designer is to give the inputs in the program for his specific layout design, give the Header Records, execute it and then the TLC file is ready for being imported into the LASI drawing window.

IV. THE ALGORITHM

The algorithm is stated below in Pseudocode:

ALGORITHM: Automated generation of layout design

```
/*  The following algorithm calculates the necessary co-ordinates needed for the  layout design and then saves those values in the predefined documented format in a TLC file so that the resulting file can directly be imported to the LASI window  */

Create TLC file with the given name;
/* Give Header Records */
INPUT name of the cell<nl>version of LASI<nl>version of TLC<nl>basic units per physical units<nl>name of physical unit<nl>date<nl>time;
INPUT Rank of Cell<sp>X of Left Outline<sp>Y of Bottom Outline<sp>X of Right Outline<sp>Y of Top Outline<nl>number of boxes<sp>paths<sp>vertices<sp>cells;
WRITE in the TLC file
        Header Records;
INPUT co-ordinates of reference point;
/* Generating Boxes */
FOR boxtype i=1 to M
{
    INPUT x_distance, y_distance,length, breadth;
    INPUT x_spacing OR y_spacing;   //For horizontally or vertically spaced boxes
    INPUT Layer_number;
        FOR each of j=1 to N boxes of type i
            CALL BOXGENERATE function;
        End FOR;
}
End FOR;
/* Generating Paths/Polygons */
FOR each of  k=1 to R paths
{
    INPUT width, Layer_number,
    x1,y1,x2,y2,x3,y3,…..,xn,yn;
```

CALL *PATHGENERATE function;*
}
End ***FOR;***
End Program;

BOXGENERATE function
IF *Boxes are spaced horizontally*
{
Bottom_left_x=f1(reference_x, x_distance,x_spacing,i, j);
Bottom_left_y=g1(reference_y, y_distance, x_spacing,i, j);
Top_right_x=h1(reference_x, x_distance , x_spacing,i, j);
Top_right_y=p1(reference_y , y_distance , x_spacing,i, j);
}
ELSE IF *Boxes are spaced vertically*
{
Bottom_left_x=f2(reference_x , x_distance , y_spacing,i, j);
Bottom_left_y=g2(reference_y , y_distance , y_spacing,i, j);
Top_right_x=h2(reference_x , x_distance , y_spacing,i, j);
Top_right_y=p2(reference_y , y_distance , y_spacing,i, j);
}
End ***IF;***
WRITE *in the TLC file*
=B <nl> Layer_number <sp> Bottom_left_x <sp> Bottom_left_y <sp> Top_right_x <sp> Top_right_y <nl>;
End BOXGENERATE function;
PATHGENERATE function
WRITE *in the TLC file*
=P <nl> Layer_number <sp> width <sp> Number_of_vertices <nl> x1 <sp> y1 <sp> x2 <sp> y2 <sp> x3 <sp> y3 <sp>….x5 <sp> y5 <nl>…..xn <sp> yn <nl>;
End PATHGENERATE function;

NOTE: <sp> = space, <nl> = newline.
x_distance => distance from the y-axis in the x direction.
y_distance => distance from the x-axis in the y direction.
Length in the x direction is labeled as ‘length’ and length in the y direction is labeled as ‘breadth’.
f1,g1,h1,p1,f2,g2,h2,p2 are functions that govern the dimension and orientation of the boxes.

V. ANALYSIS OF THE ALGORITHM

Analysis of the proposed algorithm comprises of analyzing both the time and space complexities that are given below:

A. Time Complexity Calculation

The bulk of the running time of the algorithm is consumed in generating different types of boxes and paths of different numbers. For drawing M types of boxes each of N numbers, the algorithm takes O(MN) time to execute, since each box takes O(1) time to be generated. If M and N are close to each other, the running time of the algorithm becomes $O(N^2)$. For drawing R number of paths, the algorithm takes O(R) time to write the co-ordinates of the vertices of the mask in the .tlc file. Hence, the overall time complexity of the algorithm is O(MN)+O(R), i.e. O(MN+R), which implies that the algorithm has a quadratic running time. For boxes, variation of computation time with M and N is given in Fig.1 in graphical form.

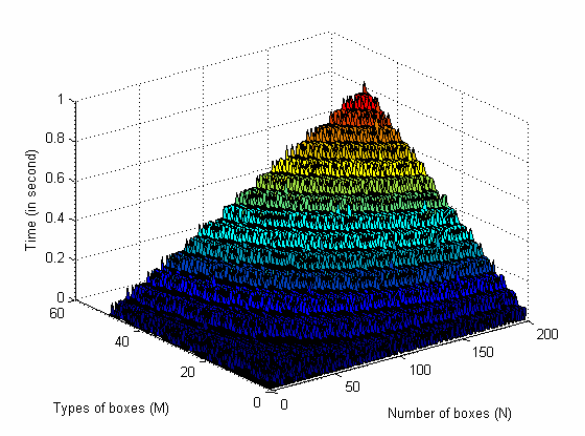

Fig. 1. Variation of computation time with M and N.

B. Space Complexity Calculation

The box generation part of the algorithm takes the dimensions (length and breadth) of the starting box, the spacing between the first two adjacent boxes and distance of the initial box from the axes as inputs. Therefore, for M types of boxes of N numbers each, the algorithm has a space complexity of O(MN). For generating R number of paths each of n sides, the space complexity of the algorithm is O(Rn). Hence, the total space complexity of the algorithm is O(MN)+O(Rn) i.e. O(MN+Rn) which implies that the algorithm has a quadratic space complexity.

VI. APPLICATION OF THE ALGORITHM

To verify the viability of the proposed algorithm it is applied to the layout design of MEMS based pressure sensors and also to the tapered design of coplanar waveguide (CPW).

A. MEMS Based Pressure Sensor

Pressure sensors are designed using the MEMS (Microelectromechanical System) technology by considering silicon as a high precision, high strength and high reliability mechanical material, that can be suitably micromachined to various mechanical structures like diaphragm, cantilevers, nozzles and grooves [10]. The present work comprises of drawing a layout for the mask of MEMS based pressure sensor using LASI by automatically creating its TLC file using the proposed algorithm. The usefulness of the proposed algorithm is evident in this case. Creating a box with length more than 2 mm was not possible in the fabrication process. So, the long box was segmented into several smaller boxes each having a dimension less than or equal to 2 mm. Also, every smaller part of the long box should have an overlapping region with its adjacent part to avoid discontinuity in the design. In order to create a TLC file containing the design of the pressure sensor mask, a turbo C program was written. The tedious task of dividing the long lines into several smaller lines with overlapping zones and calculating their coordinates was easily done by the Turbo C program. In this case, overlapping region of 50 micron was provided. The formula used for calculating the coordinates of the boxes is given below where j means box number:
For horizontally spaced boxes:

```
Bottom_left_x =reference_x + x_distance + ( j * x_spacing );
Bottom_left_y =reference_y + y_distance;
Top_right_x =Bottom_left_x + length;
Top_right_y =Bottom_left_y + breadth;
```

For vertically spaced boxes:

```
Bottom_left_x =reference_x + x_distance;
Bottom_left_y = reference_y + y_distance + ( j * y_spacing );
Top_right_x = Bottom_left_x + length;
Top_right_y = Bottom_left_y + breadth;
```

After executing the Turbo C program, a TLC file was created. Then the TLC file was successfully imported in the LASI drawing window and the design is obtained as it was expected. The details of the pressure sensor layout design produced by the C program are given in Fig. 2.

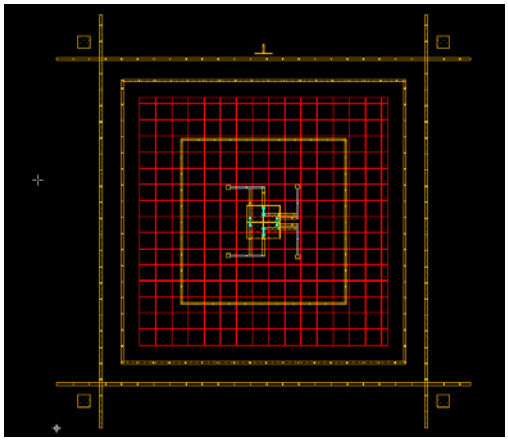

Fig. 2. Design of pressure sensor.

The coordinates of a long rectangular box comprising of 5 smaller overlapping boxes of 2 mm length each is given in Fig. 3 in exact TLC format as it is created by the program.

```
=B
 2 10000000 25262500 12000000 25462500
=B
 2 11950000 25262500 13950000 25462500
=B
 2 13900000 25262500 15900000 25462500
=B
 2 15850000 25262500 17850000 25462500
=B
 2 17800000 25262500 19800000 25462500
```

Fig. 3. TLC file generated by the program.

From Fig. 3, it is clear that the program generated the TLC file in exactly the same format as generated by hand.

B. Tapered Central Conductor Design for Coplanar Waveguide

The proposed algorithm has also been applied to the design of coplanar waveguide (CPW) for RF MEMS capacitive shunt switch in phase shifter application. Coplanar waveguides are typically used for transmission of RF signals. MEMS switches enjoy several advantages over semiconductor switches in the RF applications [12]. Using MEMS technology for RF switches one can push the cut-off frequency beyond 10,000 GHz for low-loss applications. The shunt switch is placed in shunt between the t-line and ground; and depending on the applied bias voltage, it either leaves the t-line undisturbed or connects it to ground. Details are shown in Fig. 4. But coaxial connector providing transitions to CPW are not offered by connector manufacturers [11]. The aim here is to propose a simple method of fitting standard coaxial – to – microstrip connectors with modifications as stated below. The width of the central conductor in the coplanar waveguide is quite small compared to the diameter of the SMA connector pin. So, it was intended to design such a way that interconnection between the pin and the conductor plane can be made. The CPW central conductor has been tapered to fit in with the dimensions of the signal pin of the SMA connector as illustrated in Fig. 4. Such a tapering also increases the ease of taking a contact between the signal pin of the SMA connector and the CPW central conductor. The taper has been gradually increased from a width of 100um to 700-1000um as a sinusoidal waveform so that a sharp dimension change can be avoided in order to reduce the reflection loss at the transition points.

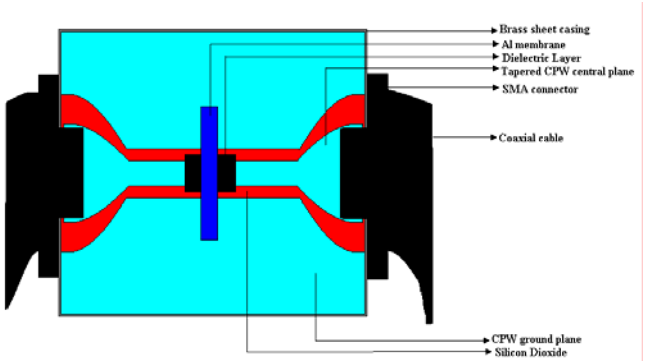

Fig. 4. Top view of the CPW structure.

To maintain 50Ω characteristic impedance throughout the transition, the gap (W) between the CPW central conductor and the ground plane is also increased as shown in Fig. 5.

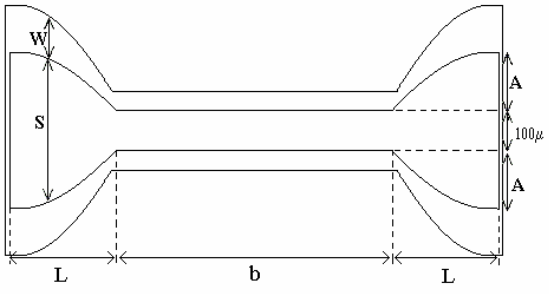

Fig. 5. Dimensions of the CPW structure.

For a given value of S, corresponding value of W needs to be calculated. The calculations can be done from the following equations that govern the characteristics of the CPW structure:

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{eff}}} \frac{K(k_0')}{K(k_0)} \quad (1)$$

$$\frac{K(k_0)}{K(k_0')} = 1 \Big/ \frac{1}{\pi} \ln\left\{2\left(\frac{1+\sqrt{k_0'}}{1-\sqrt{k_0'}}\right)\right\} \quad (2)$$

$$k_0' = \sqrt{1-k_0^2} \quad (3)$$

$$k_0 = S/(S+2W) \quad (4)$$

Taking $Z_0 = 50\Omega$, $\varepsilon_{eff} = 6.45$ and solving (1), (2), (3) and (4) it is found that :

$$W = 0.5984S \quad (5)$$

The sinusoid for the tapered shape of the central conductor is taken as $A.\sin(\omega l)$, where $\omega = \pi/2L$. Now, area of a quarter cycle of the sinusoid is $\int_0^L A.\sin(\omega x)dx = \frac{A}{\omega}$. Taking $A = 300\mu m$, $L = 6mm$ and $b = 5mm$ (figure 5) value of ω becomes 261.799 rad/m. Hence, total area of the central conductor = $6.2837 \times 10^{-6} m^2$.

The sinusoidal tapered design for the central conductor of the CPW is done by piecewise rectangular approximation as shown in Fig. 6.

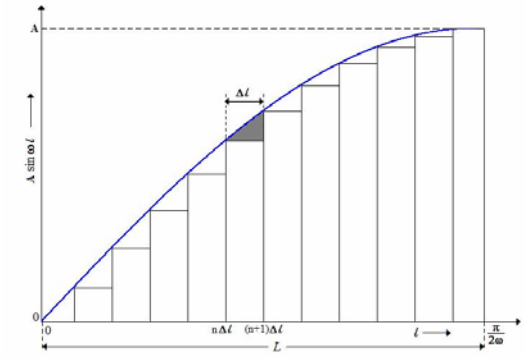

Fig. 6. Rectangular approximation of the sinusoidal shape.

Now, area of the n[th] box = $\Delta l.A.\sin(n\omega\Delta l)$. ∴ The shaded area in Fig. 6 is $\int_{n\Delta l}^{(n+1)\Delta l} A.\sin(\omega x)dx - \Delta l.A.\sin(n\omega\Delta l)$. Total error due to approximation by boxes can be found by taking the sum of all elemental errors. Hence, total deviation in area due to approximation is

$$e = \sum_{n=0}^{N-1} \left[\frac{A}{\omega}\left\{\cos\left(\omega n \frac{L}{N}\right) - \cos\left(\omega(n+1)\frac{L}{N}\right)\right\} - \frac{L}{N}.A.\sin\left(n\omega\frac{L}{N}\right) \right] \quad (6)$$

Where, N=total number of boxes= $L/\Delta l$. As $N \to \infty$, error due to approximation $\to 0$.

Percentage error is calculated with respect to the total area as:

$$\text{Percentage error} = \left(\frac{e}{6.2837 \times 10^{-6}} \times 100\right)\% \quad (7)$$

Variation of percentage error in $\log_{10}$ scale as a function of number of boxes used for approximation is shown in Fig. 7.

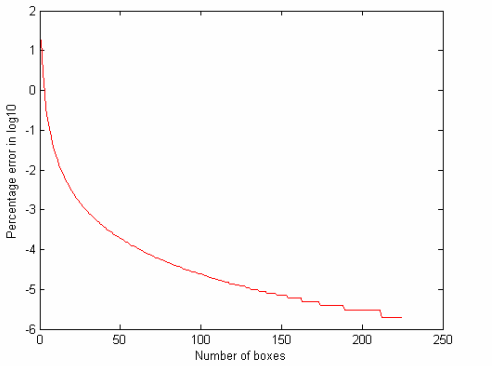

Fig. 7. Variation of percentage error with number of boxes (N)

100 small overlapping boxes were used to create the sinusoidally tapered shape of the central conductor. The formulas used in the C program for calculating the coordinates of the boxes that construct the sinusoidal taper are given below:

Bottom_left_x=reference_x+x_distance
+(box_no*x_spacing);
Bottom_left_y=reference_y+y_distance
—300*sin(261.799*box_no*$|x\_spacing|$/1000000);
Top_right_x= Bottom_left_x + length;
Top_right_y=Bottom_left_y+breadth
+2*300*sin(261.799*box_no*$|x\_spacing|$/1000000);

In the calculation of Top_right_y, 'breadth' implies initial breadth i.e. 100μm. For different values of S, corresponding values of W are calculated in the C program using relation (5). Then, the points calculated using (5) are joined by a polyline. After executing the Turbo C program, it generated the TLC file containing the coordinates of all the boxes and lines. When the TLC file is imported to the LASI environment, the layout is displayed on the computer screen as a result. The layout design is shown in Fig. 8.

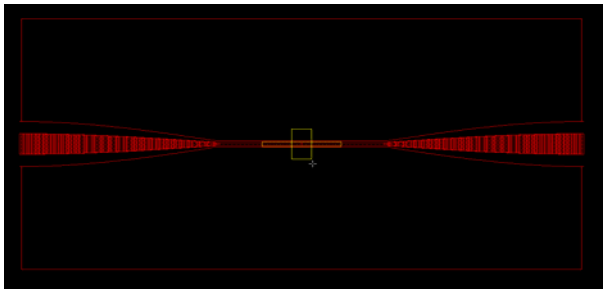

Fig. 8. Layout of the CPW with RF MEMS switch.

The resulting layout conforms to the design specifications of the CPW. The case studies presented so far testifies the applicability of the software tool developed using the proposed algorithm.

VII. CONCLUSION

The current paper focuses on the automated generation of IC mask layout using LASI. The basic intent of the work is to devise a method for layout drawing in complicated designs without manual involvement. This has been successfully done by the proposed algorithm. At the same time, the concept has been implemented using the Turbo C programming language platform. The program not only calculates the necessary parameters, it also saves those data in the well defined format in a .tlc file which is essential for directly importing the design in LASI window. The software tool developed using the algorithm has been successfully applied to generate the layout masks of MEMS based pressure sensor and coplanar waveguide. The algorithm, thus, gives a futuristic approach of layout drawing where computer programs will shoulder the responsibilities of the mask designer. Eventually it will reduce the chance of accidental errors and will save time, manpower and in turn cost of production. Further work is going on.

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IX. BIOGRAPHIES

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